JVC

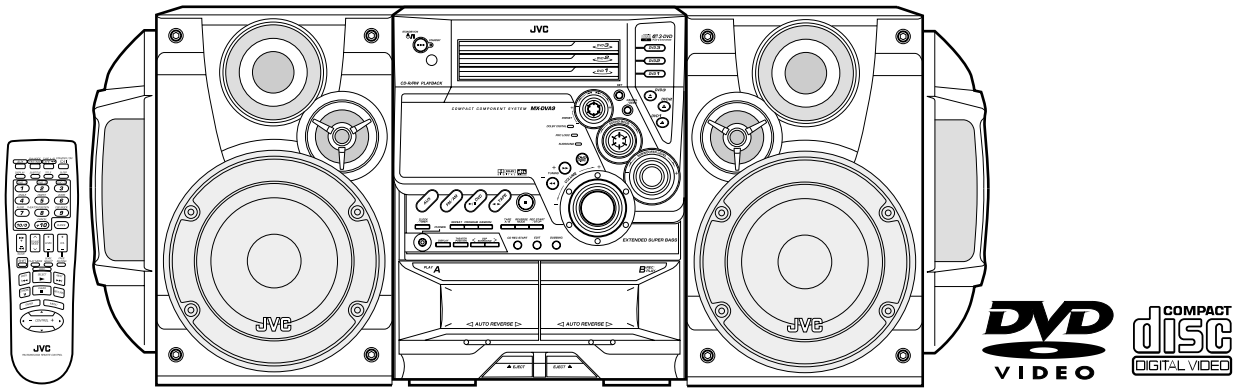
SERVICE MANUAL

COMPACT COMPONENT SYSTEM

MX-DVA9

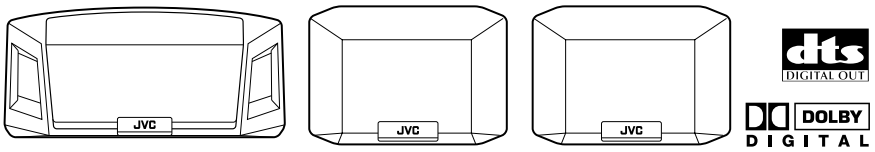
Area suffix

J ---------- U.S.A.
C ---------- Canada



SP-MXG79 CA-MXDVA9 SP-MXG79

SP-DS99TN



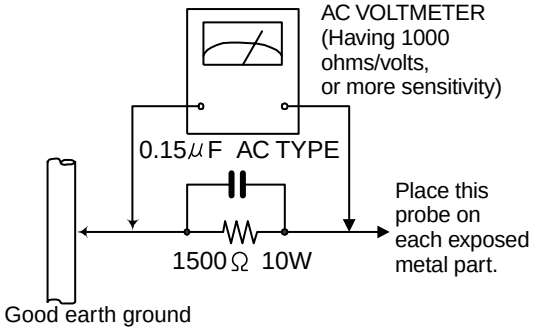
(SP-DSC99TN) (SP-DSS99TN)

Contents

No.21027
Oct. 2001

Safety Precautions

1. This design of this product contains special hardware and many circuits and components specially for safety purposes. For continued protection, no changes should be made to the original design unless authorized in writing by the manufacturer. Replacement parts must be identical to those used in the original circuits. Services should be performed by qualified personnel only.
2. Alterations of the design or circuitry of the product should not be made. Any design alterations of the product should not be made. Any design alterations or additions will void the manufacturer`s warranty and will further relieve the manufacture of responsibility for personal injury or property damage resulting therefrom.
3. Many electrical and mechanical parts in the products have special safety-related characteristics. These characteristics are often not evident from visual inspection nor can the protection afforded by them necessarily be obtained by using replacement components rated for higher voltage, wattage, etc. Replacement parts which have these special safety characteristics are identified in the Parts List of Service Manual. Electrical components having such features are identified by shading on the schematics and by (⚠) on the Parts List in the Service Manual. The use of a substitute replacement which does not have the same safety characteristics as the recommended replacement parts shown in the Parts List of Service Manual may create shock, fire, or other hazards.
4. The leads in the products are routed and dressed with ties, clamps, tubings, barriers and the like to be separated from live parts, high temperature parts, moving parts and/or sharp edges for the prevention of electric shock and fire hazard. When service is required, the original lead routing and dress should be observed, and it should be confirmed that they have been returned to normal, after re-assembling.
5. Leakage currnet check (Electrical shock hazard testing)
   After re-assembling the product, always perform an isolation check on the exposed metal parts of the product (antenna terminals, knobs, metal cabinet, screw heads, headphone jack, control shafts, etc.) to be sure the product is safe to operate without danger of electrical shock.
   Do not use a line isolation transformer during this check.
   - Plug the AC line cord directly into the AC outlet. Using a "Leakage Current Tester", measure the leakage current from each exposed metal parts of the cabinet, particularly any exposed metal part having a return path to the chassis, to a known good earth ground. Any leakage current must not exceed 0.5mA AC (r.m.s.).
   - Alternate check method
     Plug the AC line cord directly into the AC outlet. Use an AC voltmeter having, 1,000 ohms per volt or more sensitivity in the following manner. Connect a 1,500Ω 10W resistor paralleled by a 0.15μF AC-type capacitor between an exposed metal part and a known good earth ground. Measure the AC voltage across the resistor with the AC voltmeter.
     Move the resistor connection to each exposed metal part, particularly any exposed metal part having a return path to the chassis, and meausre the AC voltage across the resistor. Now, reverse the plug in the AC outlet and repeat each measurement. Voltage measured any must not exceed 0.75 V AC (r.m.s.). This corresponds to 0.5 mA AC (r.m.s.).



Warning

1. This equipment has been designed and manufactured to meet international safety standards.
2. It is the legal responsibility of the repairer to ensure that these safety standards are maintained.
3. Repairs must be made in accordance with the relevant safety standards.
4. It is essential that safety critical components are replaced by approved parts.
5. If mains voltage selector is provided, check setting for local voltage.

⚠ CAUTION

Burrs formed during molding may be left over on some parts of the chassis. Therefore, pay attention to such burrs in the case of preforming repair of this system.

In regard with component parts appearing on the silk-screen printed side (parts side) of the PWB diagrams, the parts that are printed over with black such as the resistor (▬), diode (▬) and ICP (●) or identified by the "⚠" mark nearby are critical for safety.
When replacing them, be sure to use the parts of the same type and rating as specified by the manufacturer. (Except the J and C version)

Preventing static electricity

Electrostatic discharge (ESD), which occurs when static electricity stored in the body, fabric, etc. is discharged, can destroy the laser diode in the traverse unit (optical pickup). Take care to prevent this when performing repairs.

1.1. Grounding to prevent damage by static electricity

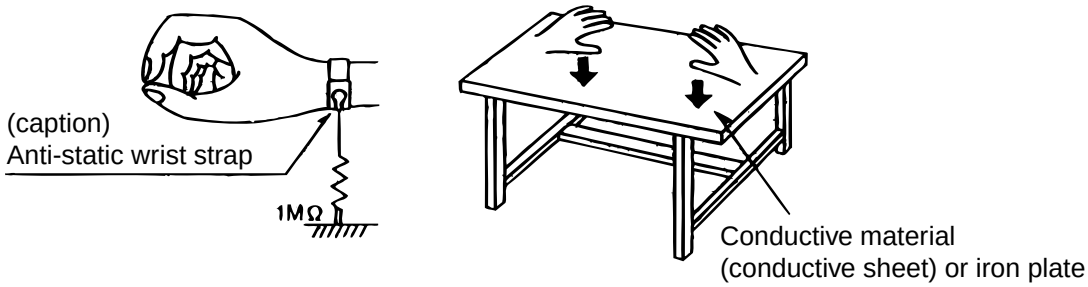
Static electricity in the work area can destroy the optical pickup (laser diode) in devices such as DVD players. Be careful to use proper grounding in the area where repairs are being performed.

1.1.1. Ground the workbench

1. Ground the workbench by laying conductive material (such as a conductive sheet) or an iron plate over it before placing the traverse unit (optical pickup) on it.

1.1.2. Ground yourself

1. Use an anti-static wrist strap to release any static electricity built up in your body.



1.1.3. Handling the optical pickup

1. In order to maintain quality during transport and before installation, both sides of the laser diode on the replacement optical pickup are shorted. After replacement, return the shorted parts to their original condition. (Refer to the next page.)

2. Do not use a tester to check the condition of the laser diode in the optical pickup. The tester's internal power source can easily destroy the laser diode.

1.2. Handling the traverse unit (optical pickup)

1. Do not subject the traverse unit (optical pickup) to strong shocks, as it is a sensitive, complex unit.

2. For specific details, refer to the replacement procedure in the text. Be careful not to take too long a time when attaching it to the connector.

3. Handle the flexible cable carefully as it may break when subjected to strong force.

4. It is not possible to adjust the semi-fixed resistor that adjusts the laser power. Do not turn it

Precautions for service

Handling of Traverse Unit and Laser Pickup

1. Do not touch any peripheral element of the pickup or the actuator.
2. The traverse unit and the pickup are precision devices and therefore must not be subjected to strong shock.
3. Do not use a tester to examine the laser diode. (The diode can easily be destroyed by the internal power supply of the tester.)
4. When replacing the pickup, after mounting a new pickup, remove the solder on the short land which is provided at the center of the flexible wire to open the circuit.
5. Half-fixed resistors for laser power adjustment are adjusted in pairs at shipment to match the characteristics of the optical block.
   Do not change the setting of these half-fixed resistors for laser power adjustment.

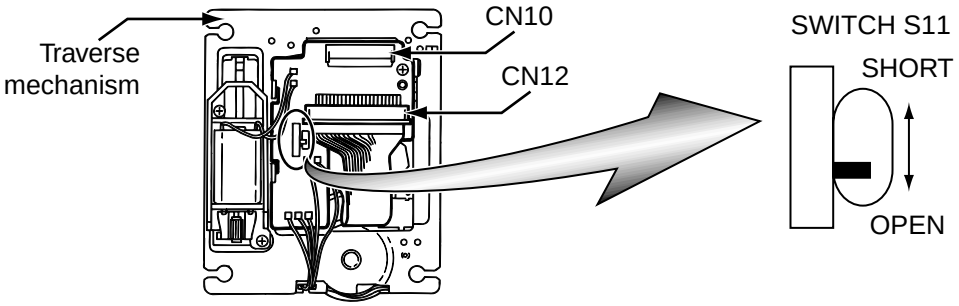
Destruction of Traverse Unit and Laser Pickup by Static Electricity

Laser diodes are easily destroyed by static electricity charged on clothing or the human body. Before repairing peripheral elements of the traverse unit or pickup, be sure to take the following electrostatic protection:

1. Wear an antistatic wrist wrap.
2. With a conductive sheet or a steel plate on the workbench on which the traverse unit or the pick up is to be repaired, ground the sheet or the plate.

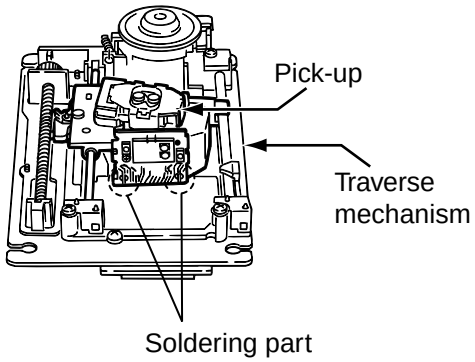
When you remove the traverse mechanism from the servo control substrate

The laser diode of pick-up might be destroyed by static electricity and set switch (S11) on the pick-up board on "SHORT" side, please before removing the card wire from connector (CN10).
Moreover, please set switch (S11) on "OPEN" side after assembling and inserting the card wire in connector (CN10) without fail at times.



When you remove the pick-up from the traverse mechanism

The laser diode of the pick-up might be destroyed by static electricity, and solder with part a, please before extracting a flexible wire from connector (CN12).
Moreover, please remove solder in part a after inserting a flexible wire in connector (CN12).



Important for laser products

1.CLASS 2a LASER PRODUCT

2.DANGER : Invisible laser radiation when open and inter lock failed or defeated. Avoid direct exposure to beam.

3.CAUTION : There are no serviceable parts inside the Laser Unit. Do not disassemble the Laser Unit. Replace the complete Laser Unit if it malfunctions.

4.CAUTION : The compact disc player uses invisible laserradiation and is equipped with safety switches whichprevent emission of radiation when the drawer is open and the safety interlocks have failed or are de feated. It is dangerous to defeat the safety switches.

5.CAUTION : If safety switches malfunction, the laser is able to function.

6.CAUTION : Use of controls, adjustments or performance of procedures other than those specified herein may result in hazardous radiation exposure.

⚠ ***CAUTION*** **Please use enough caution not to see the beam directly or touch it in case of an adjustment or operation check.**

VARNING : Osynlig laserstrålning är denna del är öppnad och spårren är urkopplad. Betrakta ej strålen.

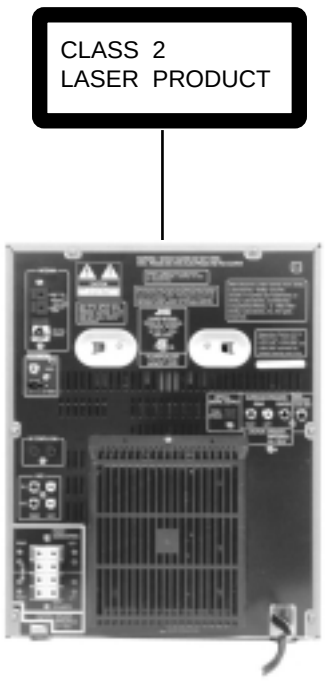
VARO : Avattaessa ja suojalukitus ohitettaessa olet alttiina näkymättömälle lasersäteilylle.Älä katso säteeseen.

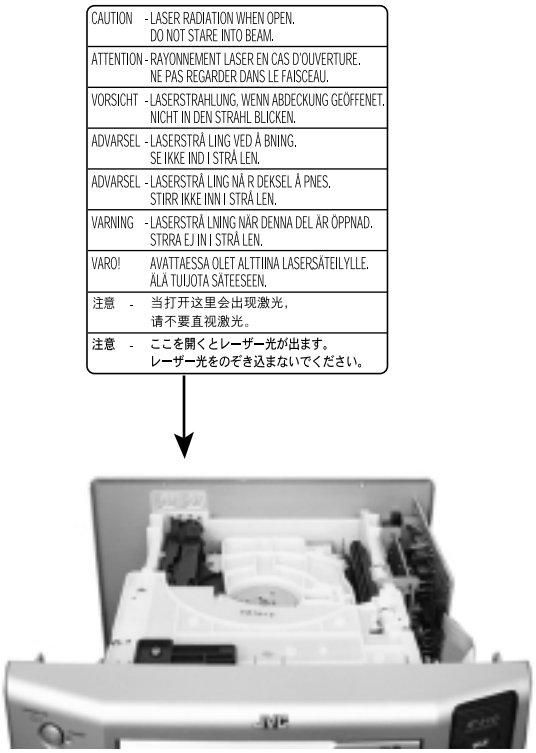
ADVARSEL : Usynlig laserstråling ved åbning , når sikkerhedsafbrydere er ude af funktion. Undgå udsættelse for stråling.

ADVARSEL : Usynlig laserstråling ved åpning,når sikkerhetsbryteren er avslott. unngå utsettelse for stråling.

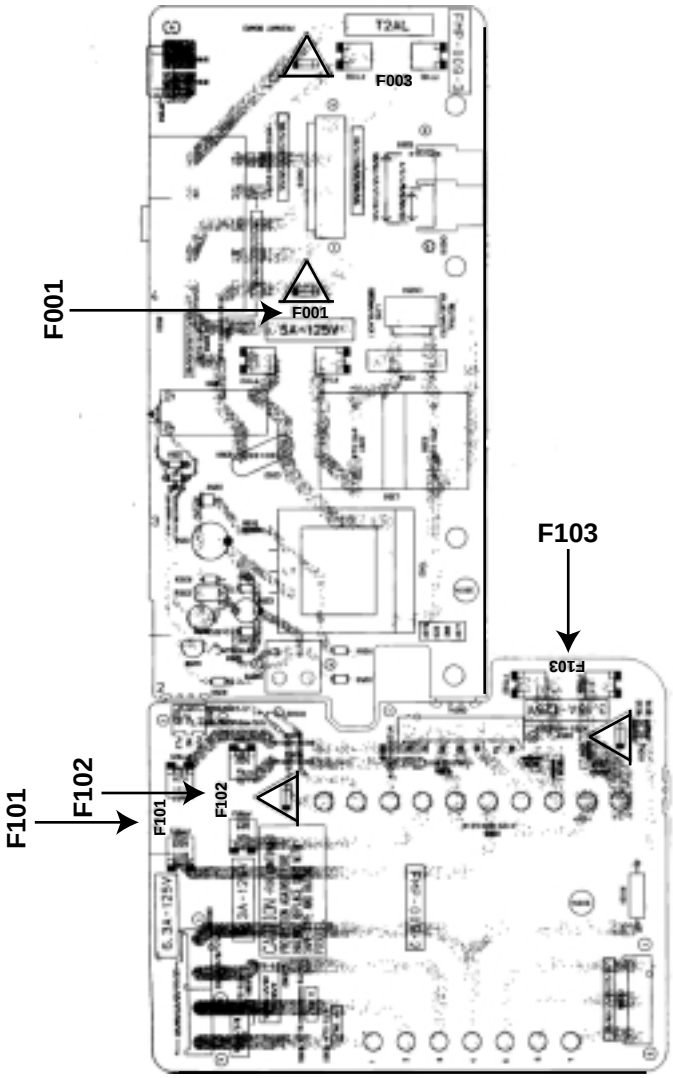
REPRODUCTION AND POSITION OF LABELS

WARNING LABEL

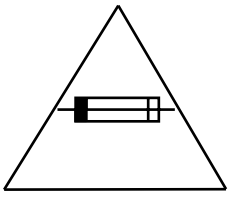




Importance administering point on the safety



For USA and Canada / pour États - Unis d' Amérique et Canada



Caution: For continued protection against risk of fire, replace only with same type 5A/125V for F001,3.15A/125V for F103,6.3A/125V for F101 and F102. This symbolspecifies type of fast operating fuse.

Precaution: Pour eviter risques de feux, remplacez le fusible de sureté de F001 comme le meme type que 5A/125V,F103 comme le meme type que 3.15A/125,et 6.3A/125V pour F101 et F102.
Ce sont des fusibles suretes qui functionnes rapide.

Disassembly method

<Main body>

■ Removing the metal cover

(See Fig.1 to 3)

1. Remove the six screws **A** on the back of the body.
2. Remove the two screws **B** on both sides of the body.
3. Remove the metal cover from the body by lifting the rear part of the cover.

CAUTION: Do not break the front panel tab fitted to the metal cover.

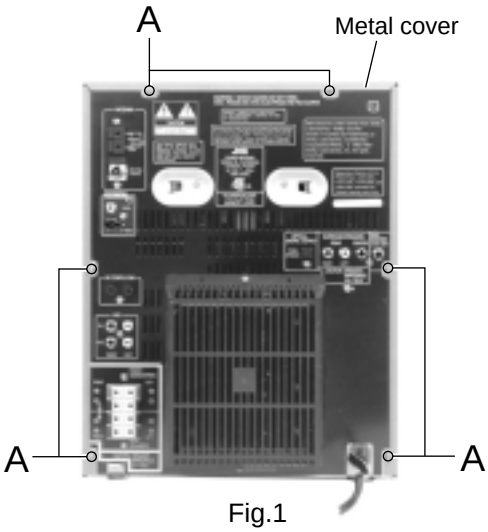


Fig.1

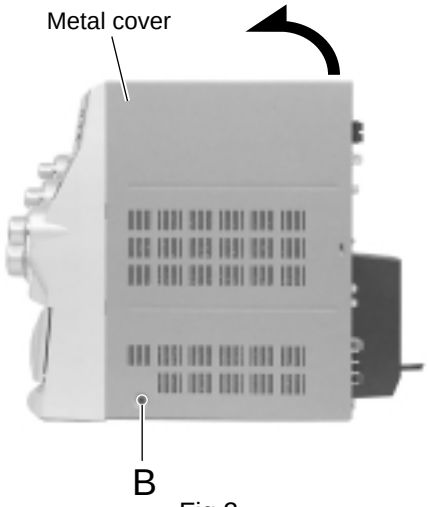


Fig.2

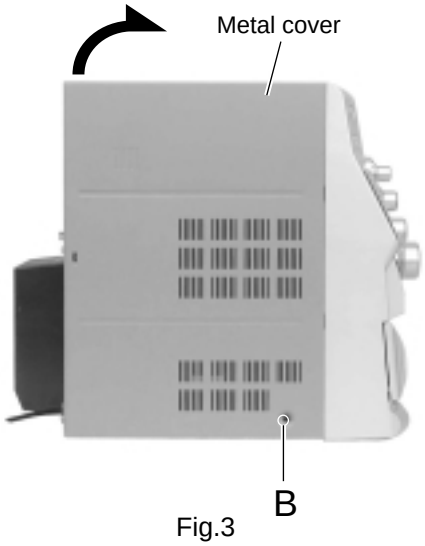


Fig.3

■Removing the DVD mechanism assembly (See Fig.4 to 7)

- Prior to performing the following procedure, remove the metal cover.

1. Disconnect the card wire from connector CN542 on the main board on the right side of the body.

2. Disconnect the wire from CN501 on the DVD servo board in the lower part of the DVD mechanism assembly, on the left side of the body.

3. Remove the screw **F** from the rear panel on the back of the body. Disconnect the earth terminal extending from the DVD changer mechanism assembly and attached to the terminal on the antenna board.

   Remove the two screws **C** on top of the body and the two screws **D** on back of the body.

   Remove the DVD changer mechanism from behind upward while pulling the front panel assembly and the rear panel outward.

REFERENCE: At this point, the two card wires in the lower part of the DVD mechanism assembly is still connected.

6. Disconnect the card wire from connector CN540 and CN541 on the inner side of the main board on the right side of the body, and remove the DVD mechanism assembly.

REFERENCE: To prevent damage to the DVD changer mechanism assembly, make sure to pull both the front panel assembly and the rear panel outward enough to remove the DVD changer mechanism assembly.

REFERENCE: To prevent damage to the DVD fitting, be sure to pull both the rear panel and the front panel assembly enough to remove the DVD changer mechanism assembly.

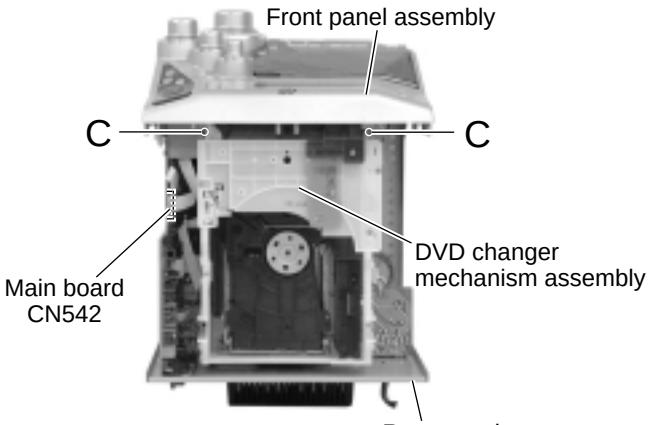


Fig.4

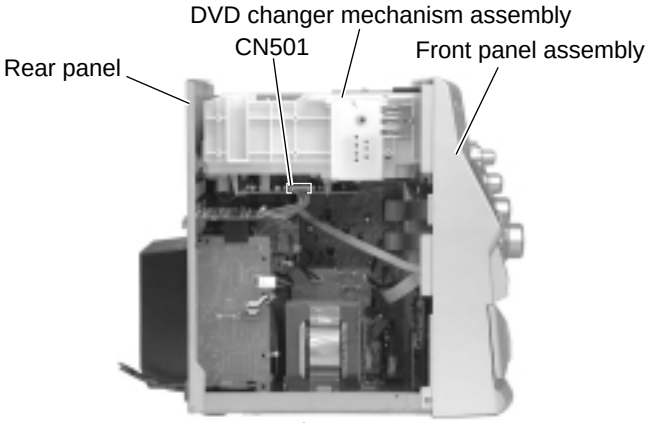


Fig.5

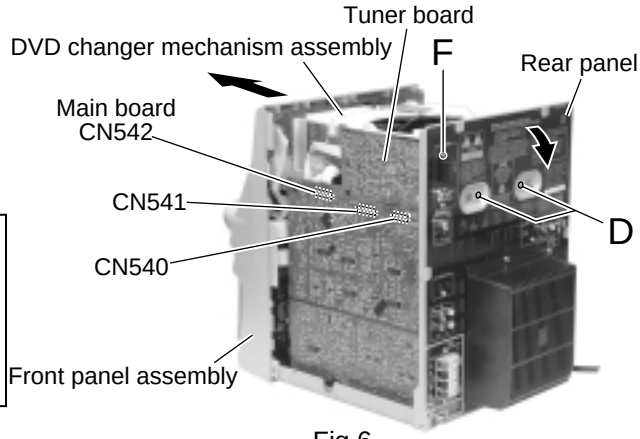


Fig.6

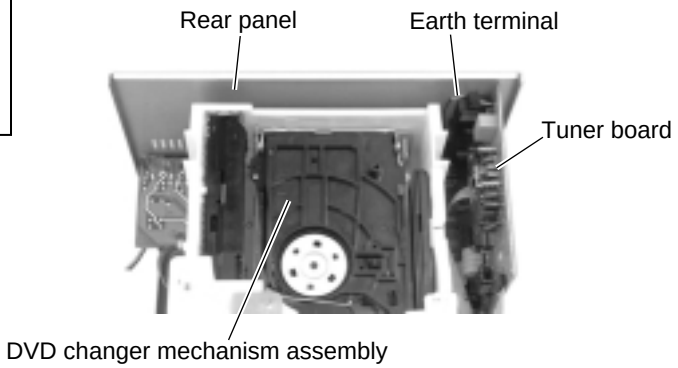


Fig.7

■ Removing the front panel assembly (See Fig.8 to 12)

- Prior to performing the following procedure, remove the metal cover and DVD changer mechanism assembly.

1. Disconnect the card wires from connector CN500, CN505 and CN510 on the main board respectively.
2. Remove the wire clamp and disconnect the wire from connector CN703 on the amplifier board.
3. Disconnect the wire from connector CN220 on the transformer board.
4. Remove the plastic rivet attaching the main board to the front assembly on the right side of the body.
5. Remove the two screws **E** on the bottom of the body.
6. Release the two joints **a** on the lower right and left sides of the body using a screwdriver, and remove the front panel assembly toward the front.

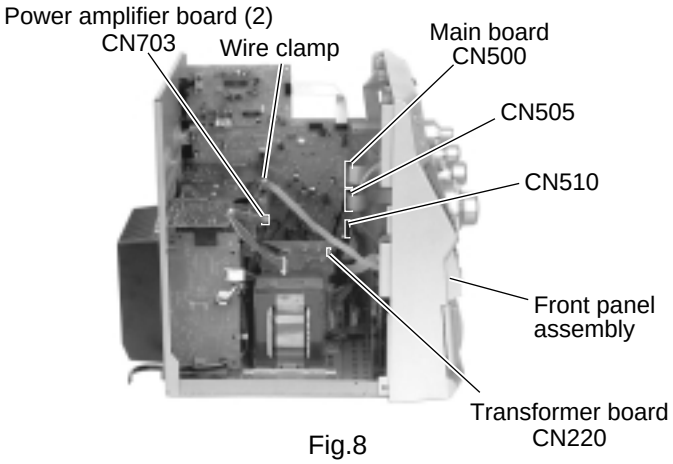


Fig.8

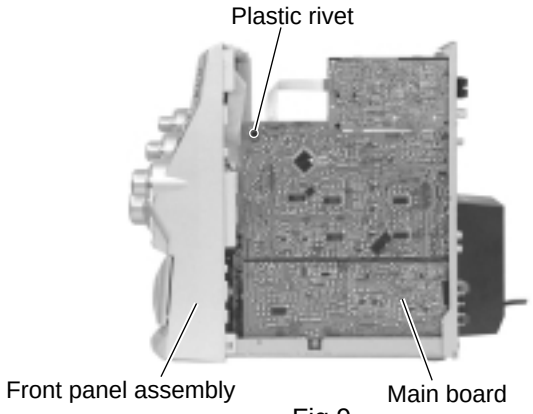


Fig.9

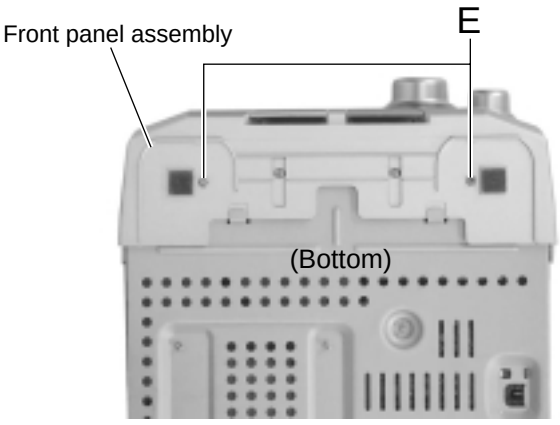


Fig.10

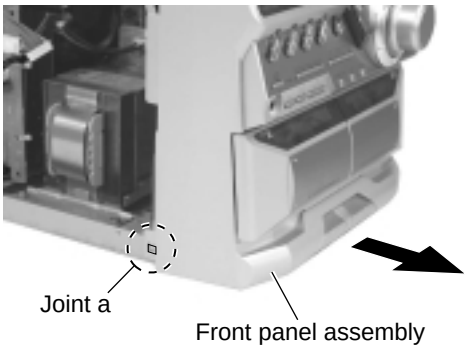


Fig.12

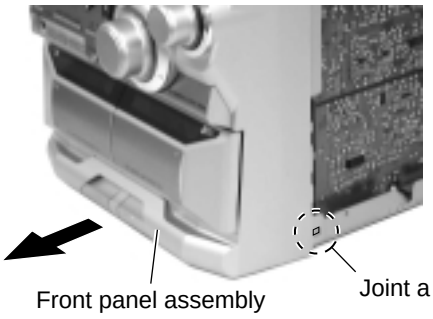


Fig.11

■ Removing the tuner board (See Fig.13 and 14)

・ Prior to performing the following procedure, remove the metal cover.

1. Disconnect the card wire from connector CN1 on the tuner board on the right side of the body.
2. Remove the plastic rivet fixing the tuner board.
3. Remove the two screws **F** on the back of the body.

CAUTION: When reassembling, connect the earth terminal which is extending from the DVD changer mechanism assembly and attached to the tuner board, to the inner side of the rear panel.

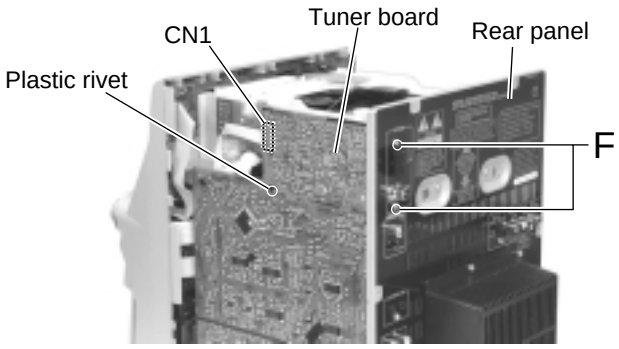


Fig.13

■ Removing the rear cover / rear panel (See Fig.15 to 17)

・ Prior to performing the following procedure, remove the metal cover and the DVD changer mechanism assembly, the tuner board.

1. Remove the screw **G** attaching the rear cover on the back of the body.
2. Push each tab of the four joints **b** in the direction of the arrow and release.
3. Remove the thirteen screws **F** attaching the rear panel.
4. Disengage the joints **c** on each lower side of the rear panel using a screwdriver and remove the rear panel backward.

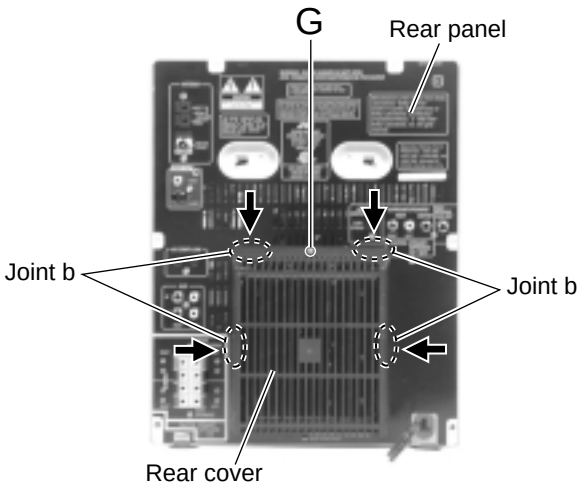


Fig.14

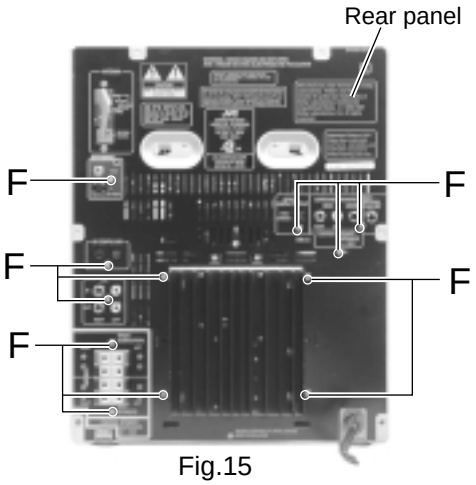


Fig.15

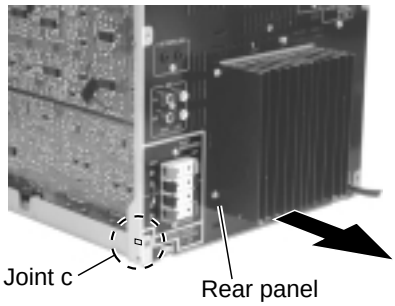


Fig.17

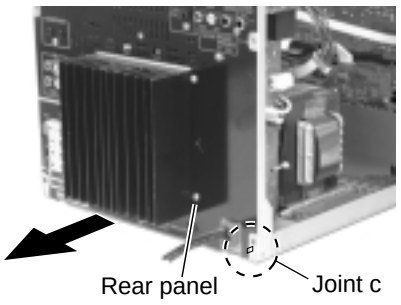


Fig.16

■Removing the main board

(See Fig.18 and 19)

・ Prior to performing the following procedure, remove the metal cover, the DVD changer mechanism assembly, the rear panel and the antenna board.

1. Disconnect the card wire from connector CN500, CN505, CN510 and the wire from CN513 on the main board respectively.

2. Remove the plastic rivet and the screw **H** attaching the main board on the right side of the body.

3. Disconnect connector CN521 on the main board from the analog output board outward. Disconnect connector CN530 and CN531 in the lower part of the main board from the regulator board upward.

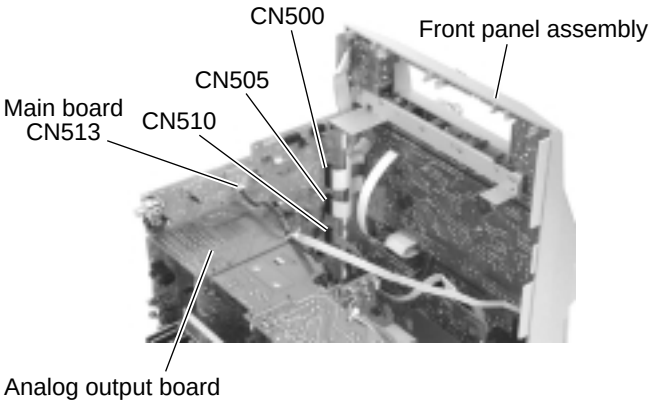


Fig.18

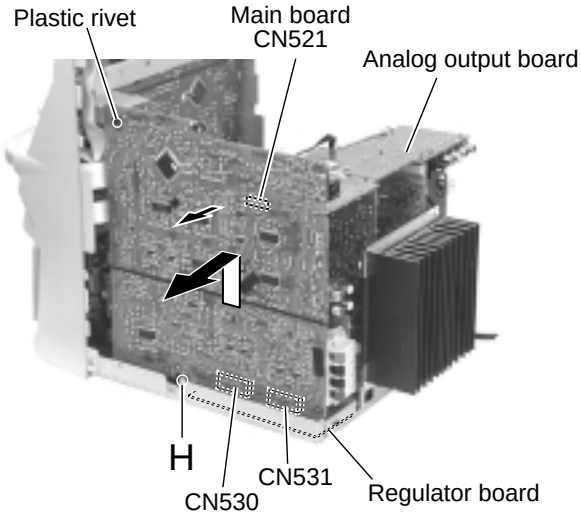


Fig.19

■Removing the speaker board

(See Fig.20)

・ Prior to performing the following procedure, remove the metal cover, the DVD changer mechanism assembly and the rear panel.

REFERENCE:	It is not necessary to remove the main board.

1. Disconnect connector CN287 on the speaker board from the regulator board.

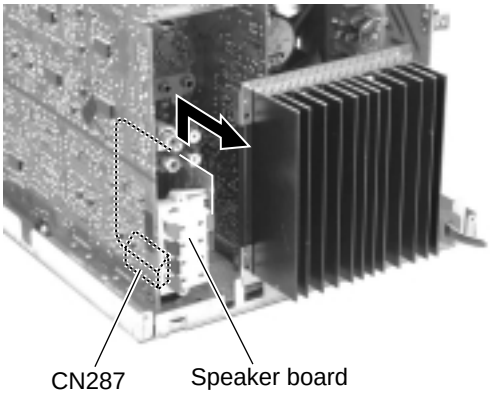


Fig.20

■ Removing the power board / power cord (See Fig.21)

・ Prior to performing the following procedure, remove the metal cover, the DVD changer mechanism assembly and the rear panel.

1. Disconnect the wire from connector CN218 on the power board.
2. Move the power cord stopper upward and remove.
3. Disconnect connector CN213 on the power board from the regulator board.
4. Remove the two wire clamps fixing the power cord and disconnect the power cord from connector CN250 on the power board.

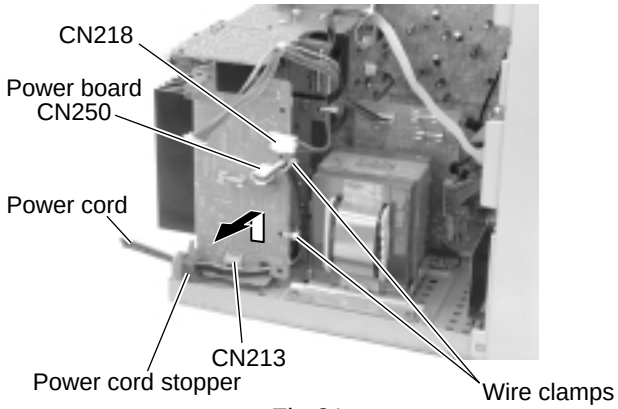


Fig.21

■ Removing the analog output board / fan (See Fig.22 to 24)

・ Prior to performing the following procedure, remove the metal cover, the DVD changer mechanism assembly, the rear panel and the antenna board.

1. Disconnect the wire from connector CN513 on the main board.
2. Remove the two wire clamps fixing the wire on the analog output board.
3. Disconnect the wire extending from the fan from connector CN705 on the power amplifier board (2).
4. Disconnect connector CN371 on the analog output board from the main board. Disconnect connector CN372 and CN373 on the analog output board from the power amplifier board (1) and the power amplifier board (2) respectively upward.
5. Remove the two screws **I** and the fan from the fan bracket.

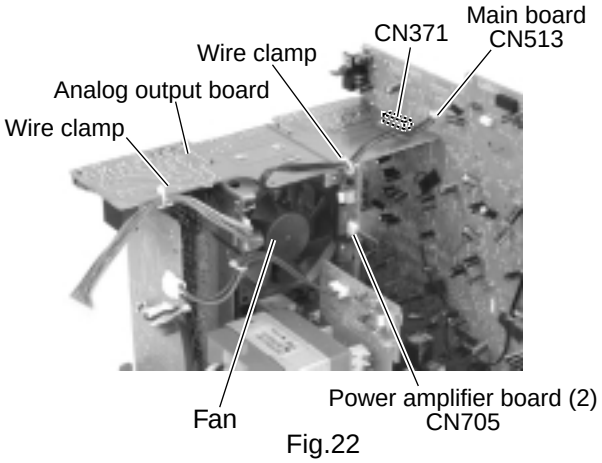


Fig.22

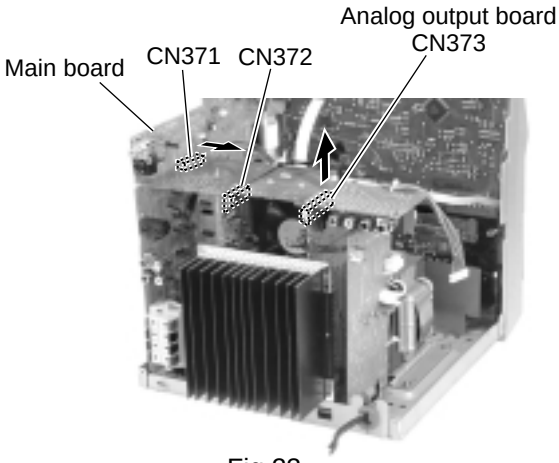


Fig.23

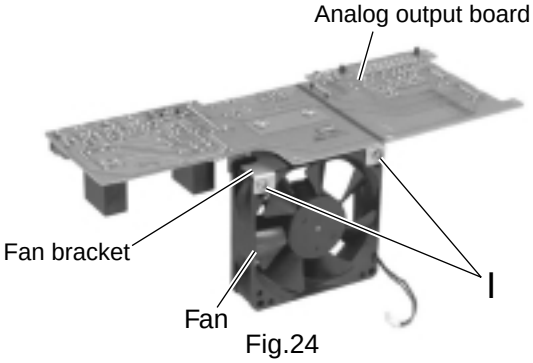


Fig.24

■ Removing the power amplifier board (1) / power amplifier board (2) / heat sink (See Fig.25 to 27)

- Prior to performing the following procedure, remove the metal cover, the DVD changer mechanism assembly, the rear panel, the antenna board and the analog output board.

1. Disconnect the wire from connector CN513 on the main board.

2. Remove the wire clamp on the power amplifier board (1).

3. Disconnect the wire from connector CN703 on the power amplifier board (2).

4. Disconnect connector CN310 on the power amplifier board (1) and CN701 on the power amplifier board (2) from the regulator board upward. The heat sink is detached with the power amplifier board (1) and the power amplifier board (2).

5. Pull out the upper and lower heat sink brackets from the heat sink.

6. Remove the four screws **J** attaching the power amplifier board (1) to the heat sink.

7. Remove the four screws **K** attaching the power amplifier board (2) to the heat sink.

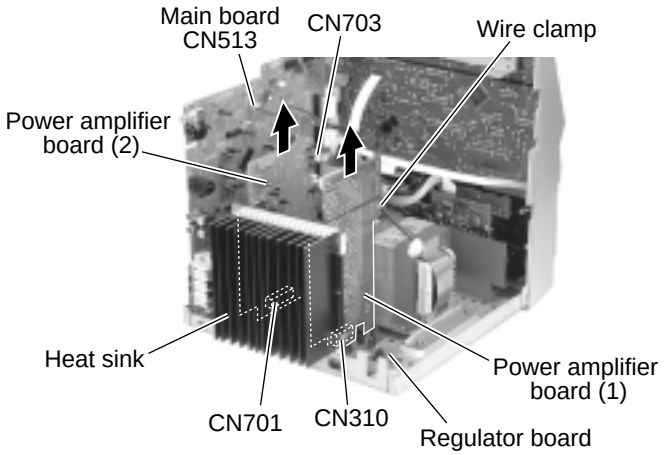


Fig.25

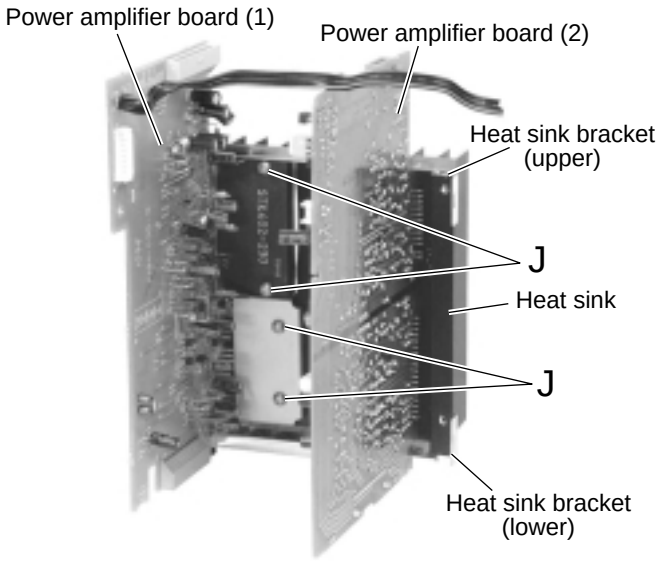


Fig.26

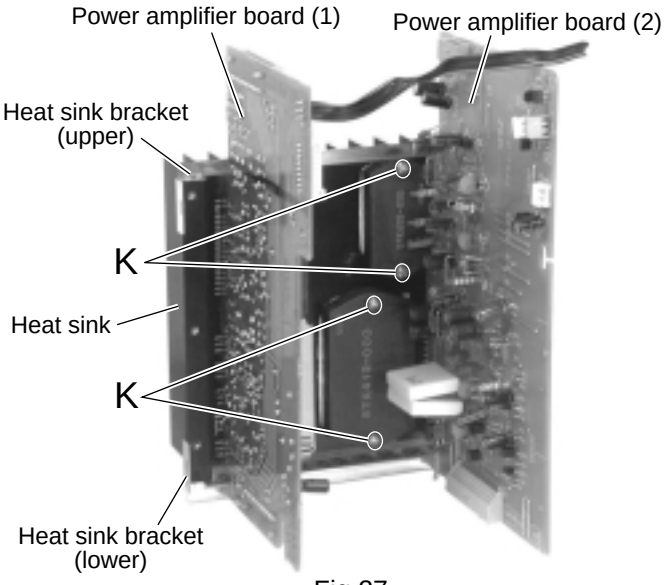


Fig.27

■ Removing the power transformer assembly (See Fig.28 and 29)

- Prior to performing the following procedure, remove the metal cover, the DVD changer mechanism assembly and the rear panel.

1. Disconnect the wire from connector CN218 on the power board.
2. Remove the wire clamp on the power amplifier board (1).
3. Disconnect the wire from connector CN204 on the regulator board.
4. Disconnect the wire from connector CN220 on the transformer board.
5. Remove the four screws **L** attaching the power transformer assembly.

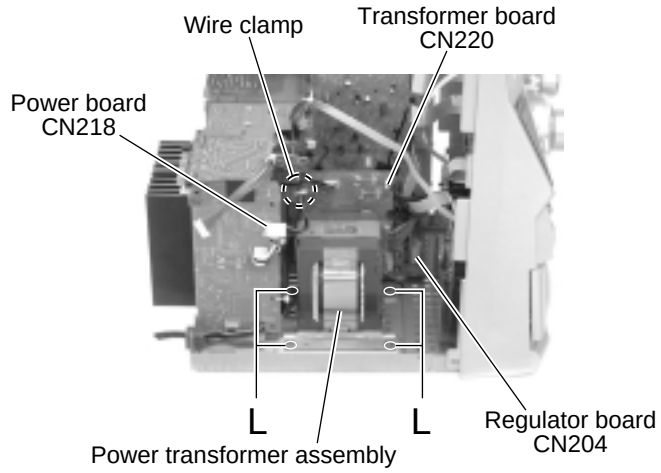


Fig.28

■ Removing the regulator board (See Fig.30)

- Prior to performing the following procedure, remove the metal cover, the DVD changer mechanism assembly, the rear panel, the antenna board, the main board, the analog output board, the power board, the power amplifier board (1), the power amplifier board (2) and the speaker board.

1. Disconnect the wire from connector CN204 on the regulator board.
2. Remove the two screws **M**.

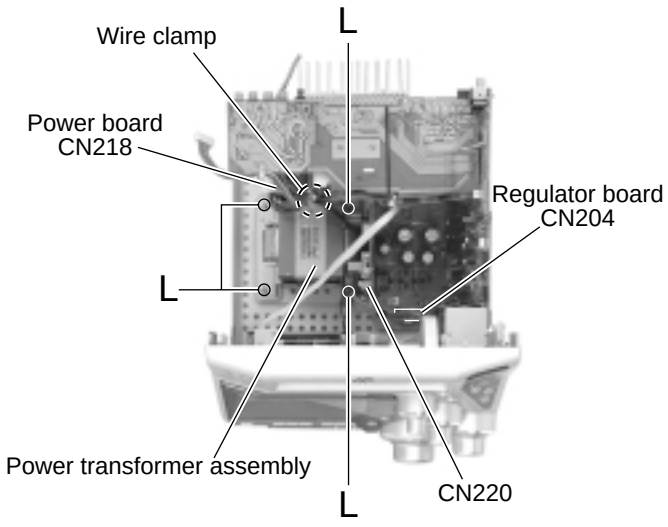


Fig.29

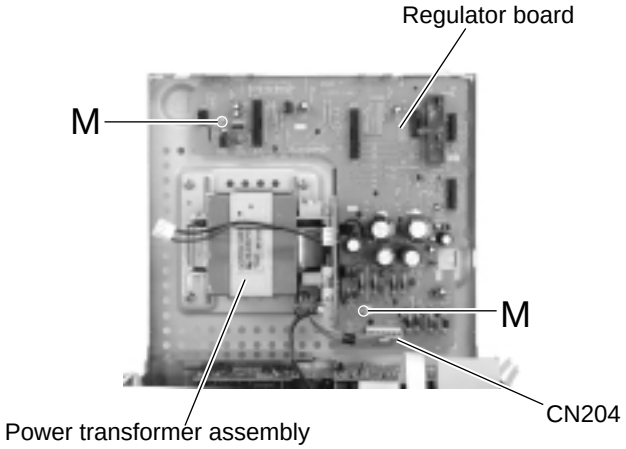


Fig.30

<Front panel assembly>

・ Prior to performing the following procedure, remove the metal cover, the DVD changer mechanism assembly and the front panel assembly.

■Removing the cassette mechanism assembly (See Fig.31)

1. Disconnect the card wire from connector CN306 on the head amplifier & mechanism control board.

2. Remove the seven screws **N** attaching the cassette mechanism assembly.

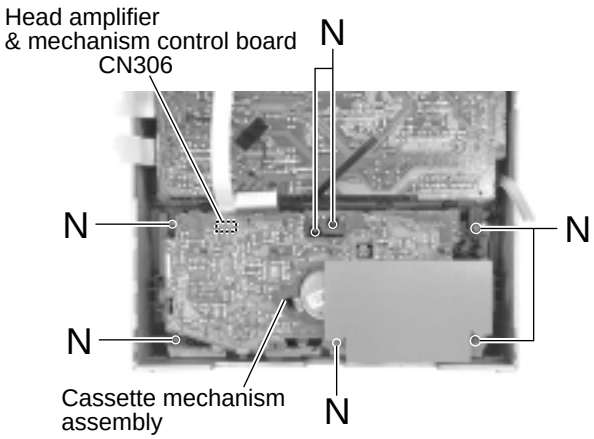


Fig.31

■Removing the display system control board (See Fig.32 to 34)

1. Remove the five screws **O** attaching the stay bracket.

2. Disconnect the card wires from connector CN316 and CN881 on the display system control board.

3. Remove the six screws **P** attaching the display system control board.

4. If necessary, disconnect the wire from connector CN870 on the front side of the display system control board and unsolder FW915.

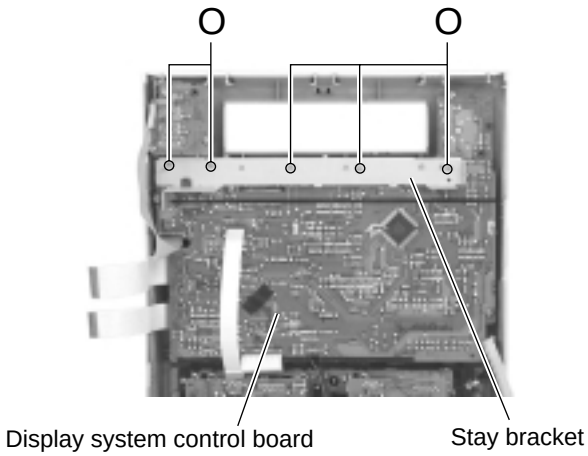


Fig.32

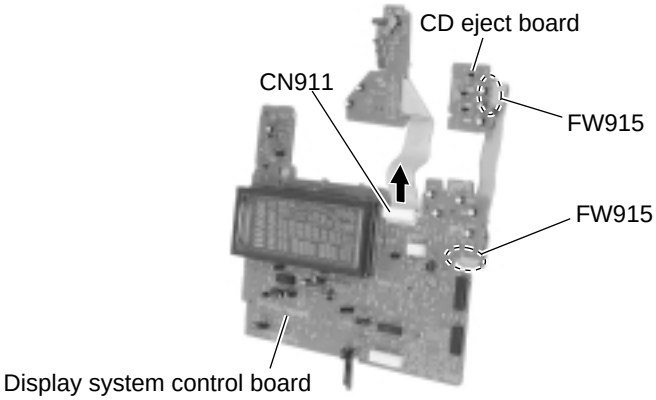


Fig.34

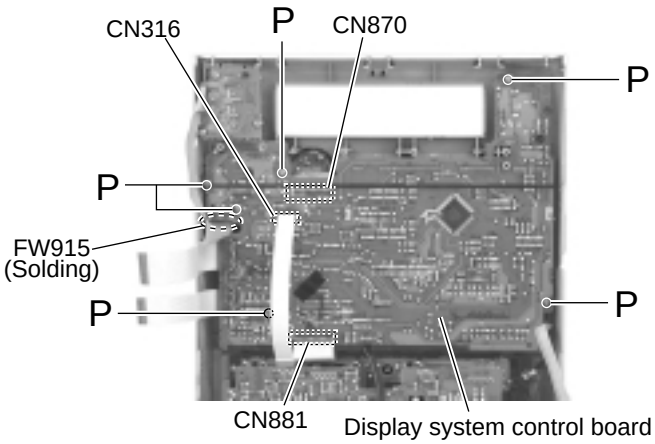


Fig.33

■ Removing the CD eject board (See Fig.35)

1. Remove the three screws **Q** attaching the DVD eject board.
2. If necessary, unsolder FW915 on the DVD eject board.

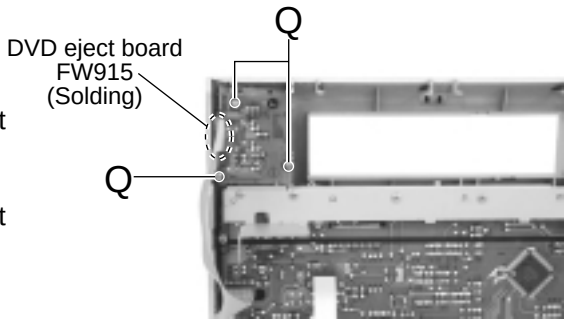


Fig.35

■ Removing the preset / tuning switch board (See Fig.36 and 37)

・ Prior to performing the following procedure, remove the display system control board.

1. Pull out the preset knob on the front panel.
2. Remove the five screws **R** attaching the preset / tuning switch board.
3. If necessary, unsolder FW901 on the preset / tuning switch board.

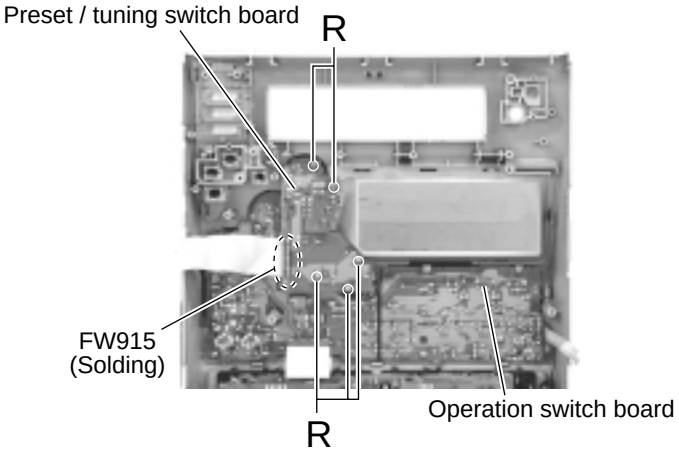


Fig.36

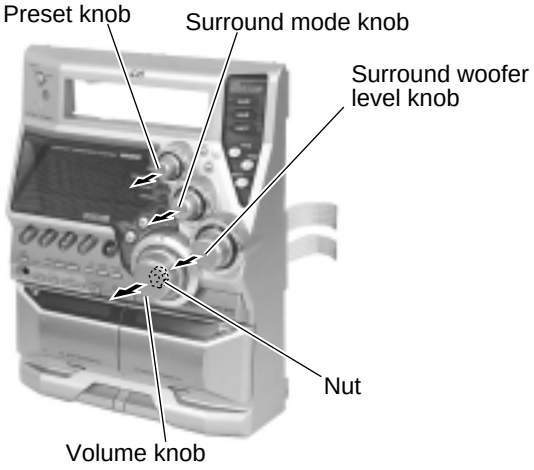


Fig.37

■ Removing the operation switch board (See Fig.37 and 38)

・ Prior to performing the following procedure, remove the display system control board and the preset / tuning switch board.

1. Pull out the volume knob on the front panel and remove the nut. Pull out the surround mode knob and the surround woofer level knob toward the front.
2. Remove the eleven screws **S** attaching the operation switch board.
3. Release each tab of the seven joints **g** retaining the operation switch board.

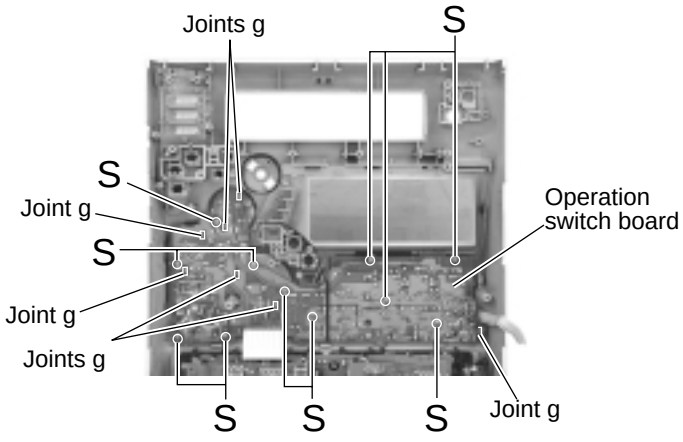


Fig.38

<DVD Changer Mechanism Section>

■Removing the DVD Servo control board

1. Remove the Metal cover.
2. Remove the DVD changer mechanism assembly.
3. From bottom side the DVD changer mechanism assembly, remove the one screw 1 retaining the DVD Servo control board.
4. Ciconnect the card wire,From the connectors CN101 and CN102, on the DVD Servo control board.

5. Disengage the two engagements "A" , remove the DVD Servo control board.

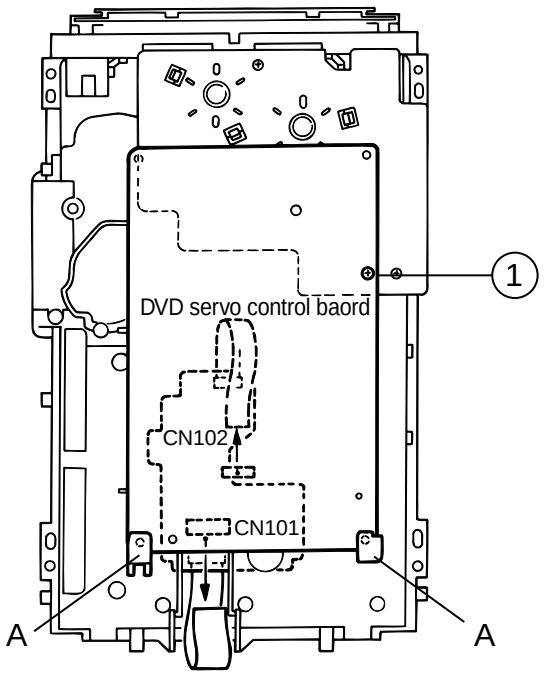


Fig.1

■Removing the DVD tray assembly (See Fig.2~4)

1. Remove the front panel assembly.
2. Remove the DVD changer mechanism assembly.
3. Remove the DVD Servo control board.
4. Remove the screw 2 retaining the Disc stopper (See Fig.3).
5. Remove the three screws 3 retaining the T.bracket (See Fig.3).
6. From the clamper base section "C" , remove both of the edges fixing the rod(See Fig.2 and 3).
7. Remove the screw 4 retaining the clamper assembly (See Fig.3).
8. From the left side face of the chassis assembly, remove the one screw 5 retaining both of the return spring and lock lever(See Fig. 4).
9. By removing the pawl at the section "D" fixing the return spring, dismount the return spring(See Fig.4).
10. Remove the three lock levers(See Fig.4).

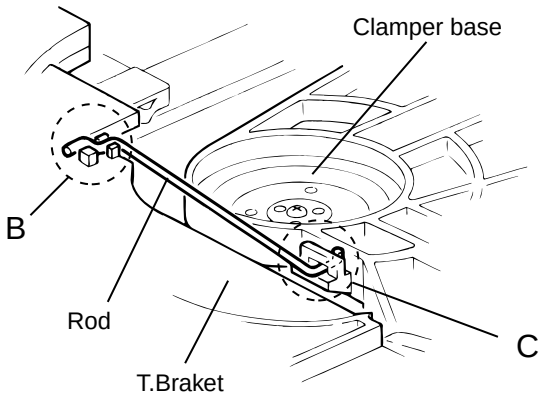


Fig.2

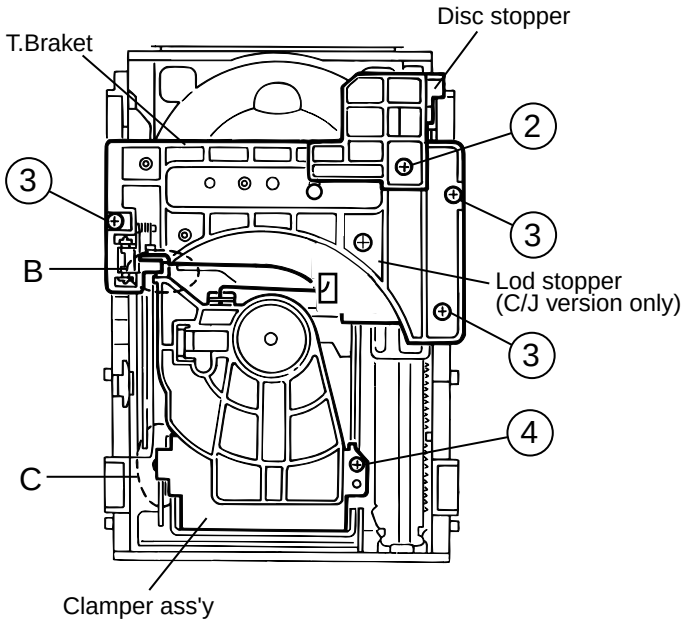


Fig.3

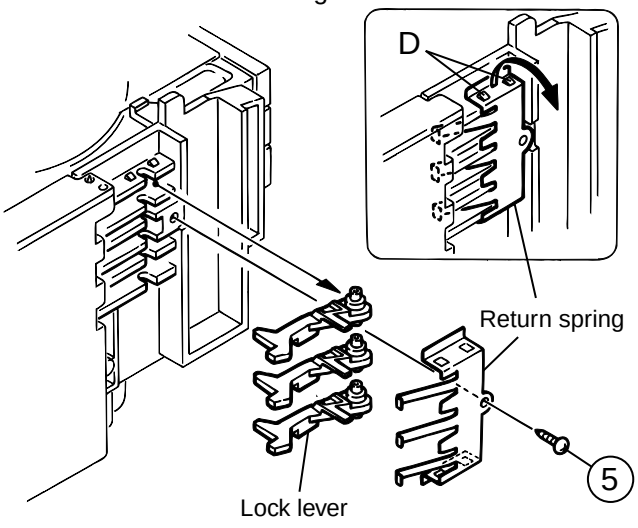


Fig.4

11. Check whether the lifter unit stopper has been caught into the hole at the section "E" of DVD tray assembly as shown in Fig.5.
12. Make sure that the driver unit elevator is positioned as shown in Fig.6 from to the second or fifth hole on the left side face of the DVD Traverse mechanism assembly.

[Caution] In case the driver unit elevator is not at above position, set the elevator to the position as shown in Fig.7 by manually turning the pulley gear as shown in Fig.8.

13. Manually turn the motor pulley in the clockwise direction until the lifter unit stopper is lowered from the section "E" of DVD tray assembly(See Fig.8).
14. Pull out all of the three stages of DVD tray assembly in the arrow direction "F" until these stages stop (See Fig.6).
15. At the position where the DVD tray assembly has stoppend, pull out the DVD tray assembly while pressing the two pawls "G and G' " on the back side of DVD tray assembly(See Fig.9). In this case, it is easy to pull out the assembly when it is pulled out first from the stage DVD tray assembly.

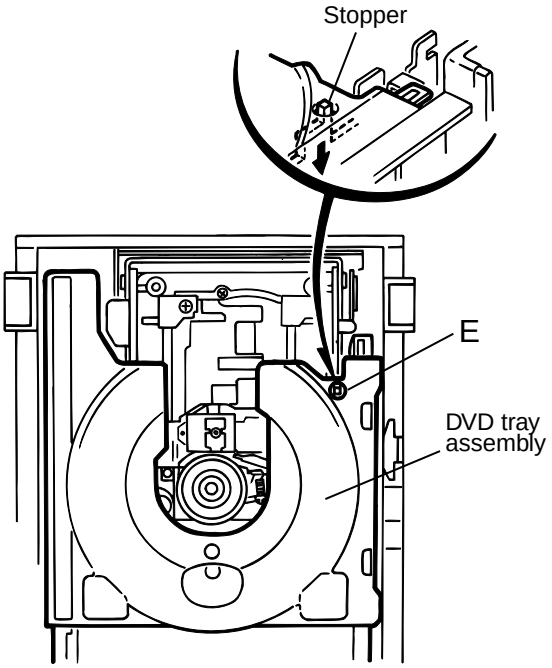


Fig.5

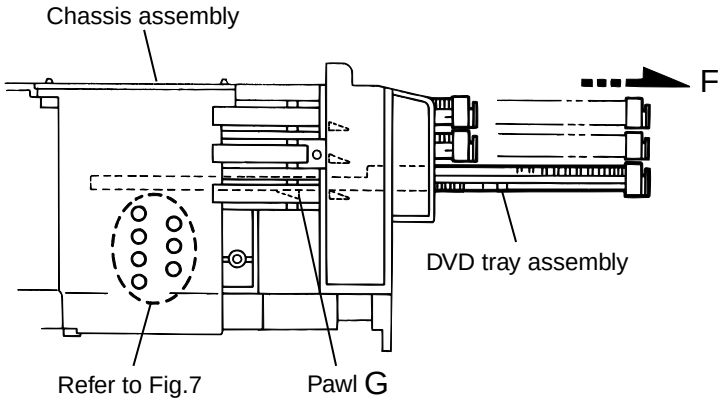


Fig.6

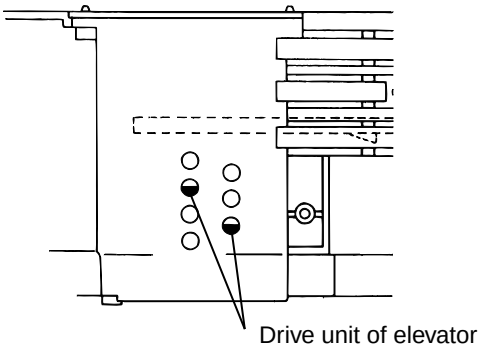


Fig.7

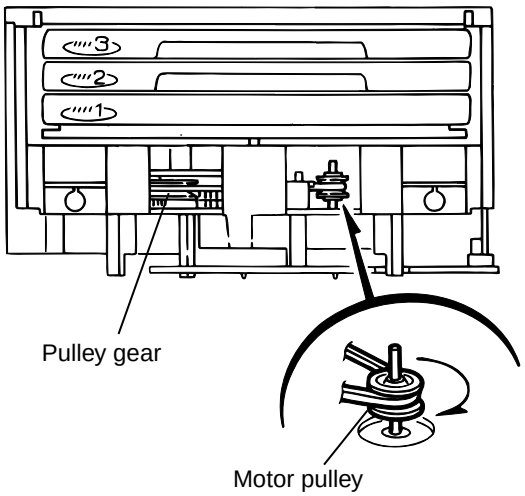


Fig.8

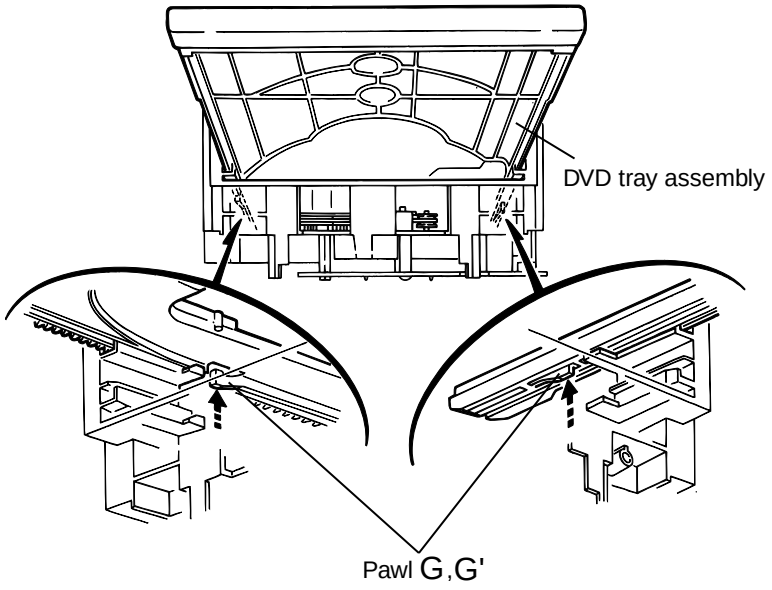


Fig.9

■Removing the DVD mechanism assembly(See Fig.10)

1. While turning the cams R1 and R2 assembly in the arrow direction "H" . align the shaft "I" of the DVD mechanism assembly to the position shown in Fig.10.
2. Remove the four screw 6 retaining the DVD mechanism assembly.

■Removing the DVD mechanism (See Fig.11 and 12)

1. For dismounting only the DVD machanism without removing the DVD mechanism assembly, align the shaft "J" of the DVD mechanism assembly to the position shown Fig.11 while turning the cam R1 and R2 assembly in the arrow direction "K" .
2. By raising the DVD mechanism assembly in the arrow direction "L" , remove the assembly from the lifter unit (See Fig.12).

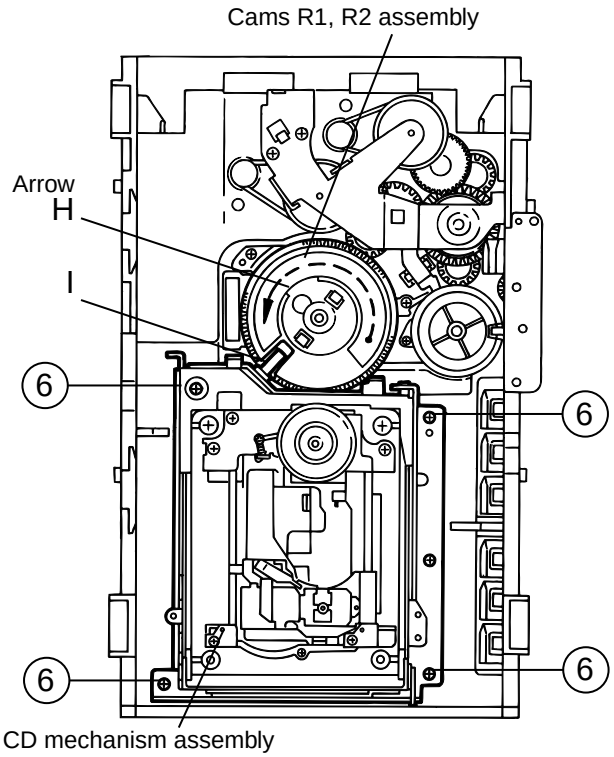


Fig.10

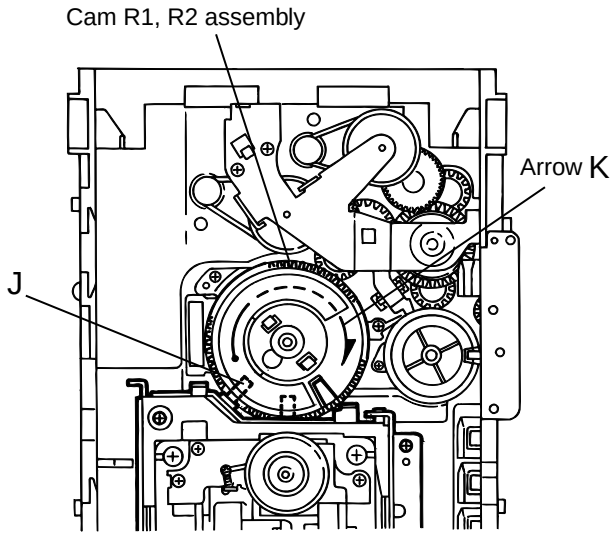


Fig.11

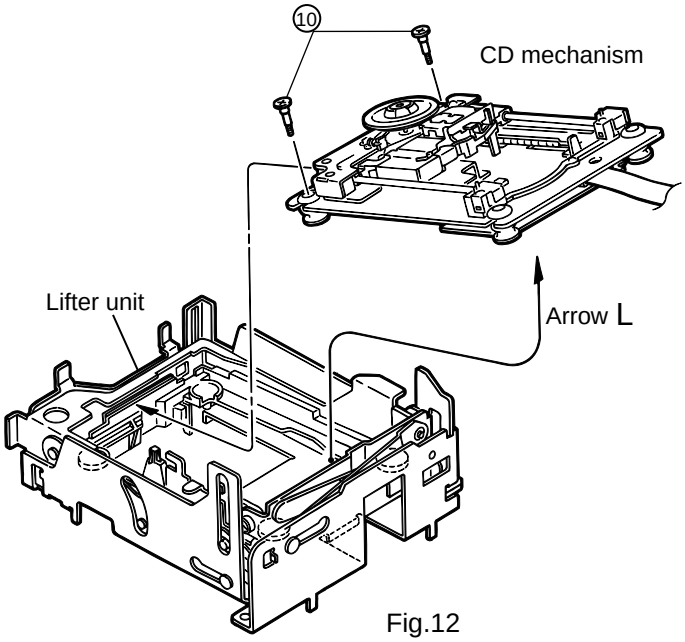


Fig.12

■Removing the actuator motor boad (See Fig.14, 15)

1. Absord the four soldered positions "M" of the right and left motors with a soldering absorber(See Fig.14).
2. Remove the two screws 7 retaining the actuator motor board(See Fig.14).
3. Remove the two screws 8 retaining the tray select switch board(See Fig.15).

■Removing the can unit (See Fig.15~18)

1. Remove the CD mechanism assembly.
2. While turning the cam gear L, align the pawl "N" position of the drive unit to the notch position(Fig.15) on the cam gear L.
3. Pull out the drive unit and cylinder gear(See Fig.17).
4. While turning the cam gear L, align the pawl "O" position of the select lever to the notch position(Fig.18) on the cam gear L.
5. Remove the four screws 9 retaining the cam unit(cam gear L and cams R1/R2 assembly)(See Fig.18).

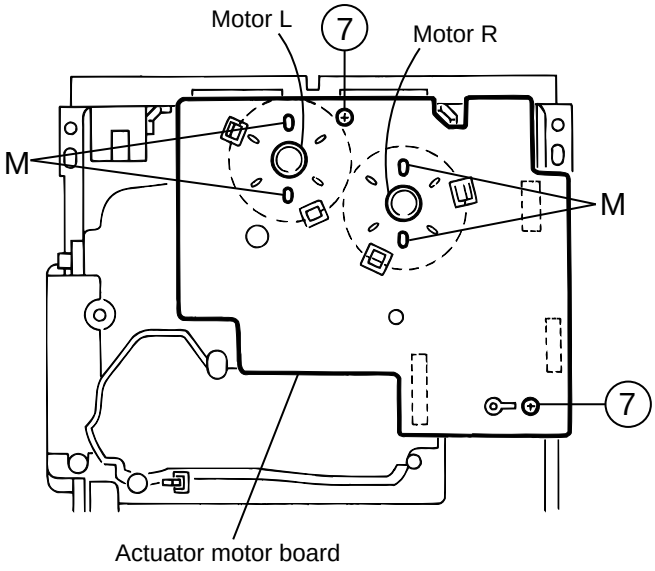


Fig.14

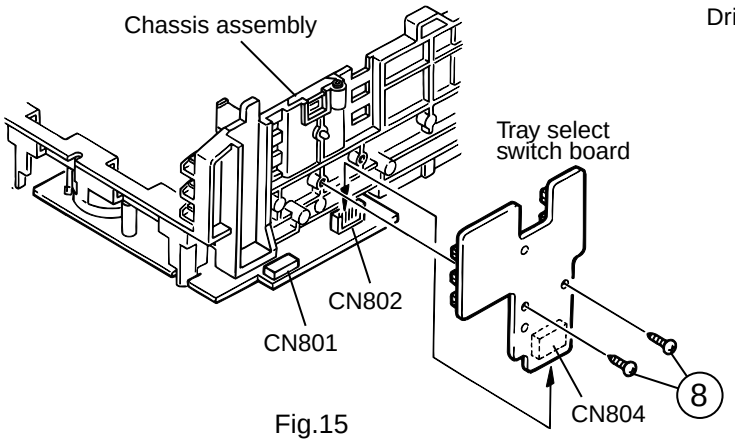


Fig.15

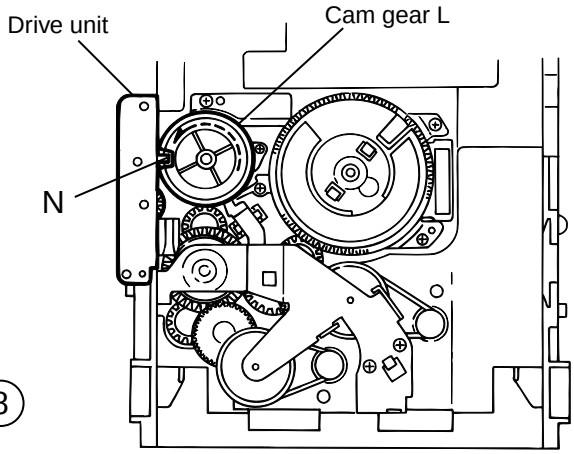


Fig.16

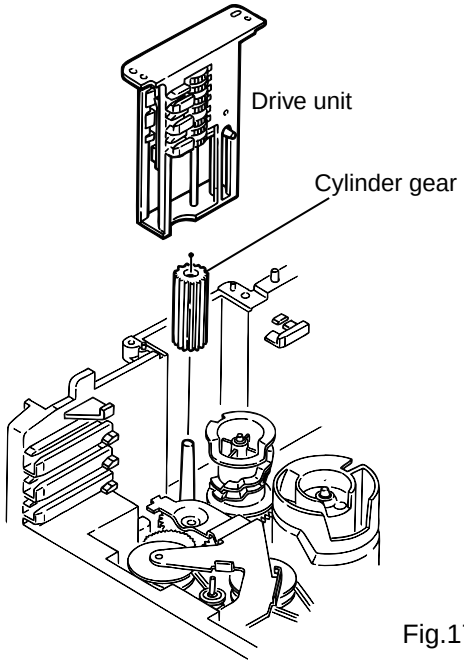


Fig.17

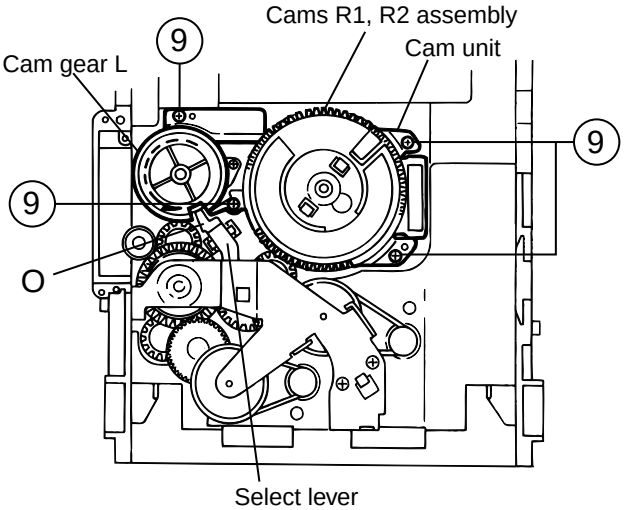


Fig.18

■ Removing the actuator motor and belt (See Fig.19~22)

1. Remove the two screws 10 retaining the gear bracket (See Fig.19).
2. While pressing the pawl "P" fixing the gear bracket in the arrow direction, remove the gear bracket (See Fig.19).
3. From the notch "Q section" on the chassis assembly fixing the edge of gear bracket, remove and take out the gear bracket(See Fig. 20).
4. Remove the belts respectively from the right and left actuator motor pulleys and pulley gears(See Fig. 19).
5. After turning over the chassis assembly, remove the actuator motor while spreading the four pawls "R" fixing the right and left actuator motors in the arrow direction(See Fig. 21).

[Note] When the chassis assembly is turned over under the conditions wherein the gear bracket and belt have been removed, then the pulley gear as well as the gear, etc. constituting the gear unit can possibly be separated to pieces. In such a case, assemble these parts by referring to the assembly and configuration diagram in Fig. 22.

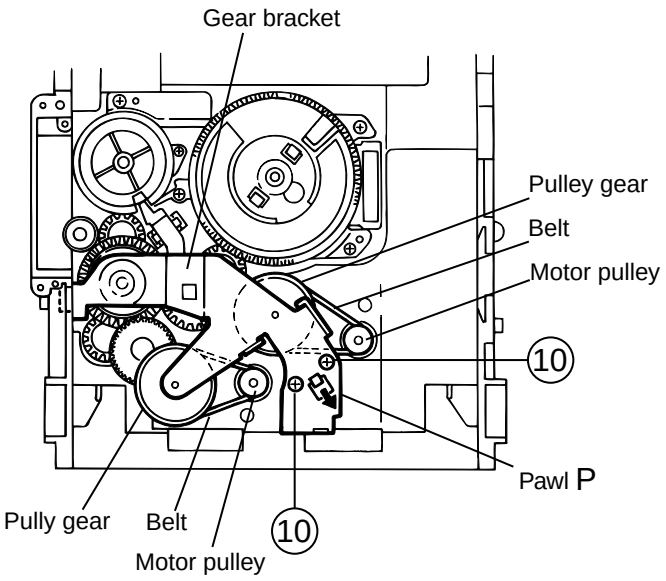


Fig.19

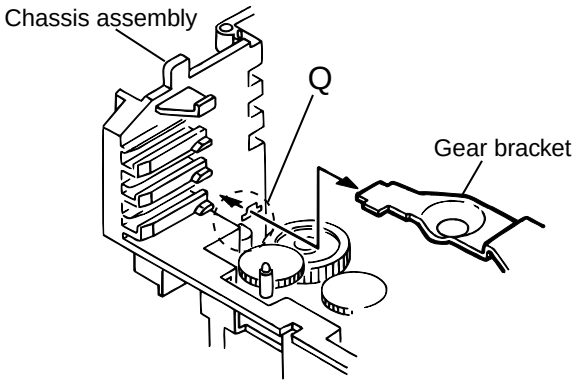


Fig.20

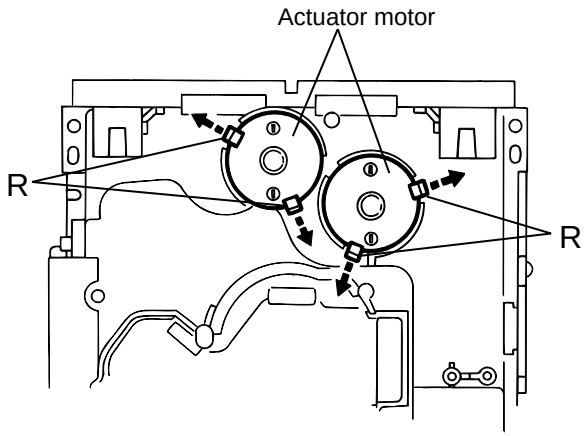


Fig.21

Assembly and Configuration Diagram

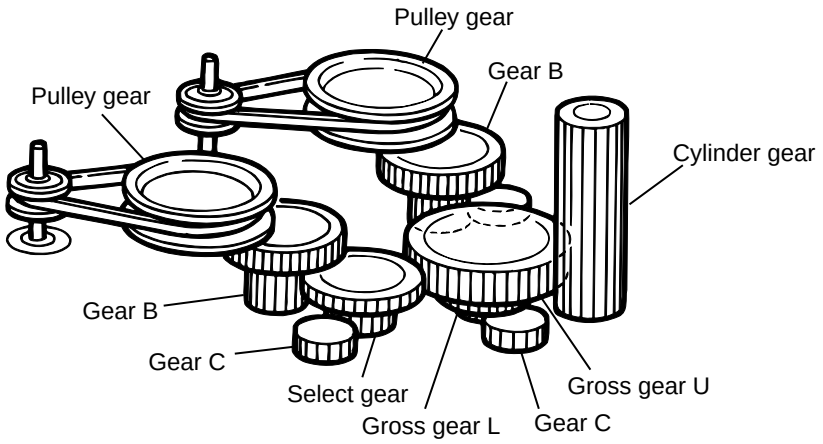


Fig.22

■ Removing the cams R1/R2 assembly and cam gear L(See Fig.23)

1. Remove the slit washer fixing the cams R1 and R2 assembly.
2. By removing the two pawls "S" fixing the cam R1, separate R2 from R1.
3. Remove the slit washer fixing the cam gear L.
4. Pull out the cam gear L from the C.G. base assembly.

■ Removing the C.G. base assembly (See Fig.23 and 24)

Remove the three screws 11 retaining the C.G. base assembly.

[Caution] To retassemble the cylinder gear, etc.with the cam unit (cam gear and cans R1/R2 assembly), gear unit and drive unit, align the position of the pawl "N" on the drive unit to that o f the notch on the cam gear L. Then, make sure that the gear unit is engaged by turning the cam gear L (See Fig. 24).

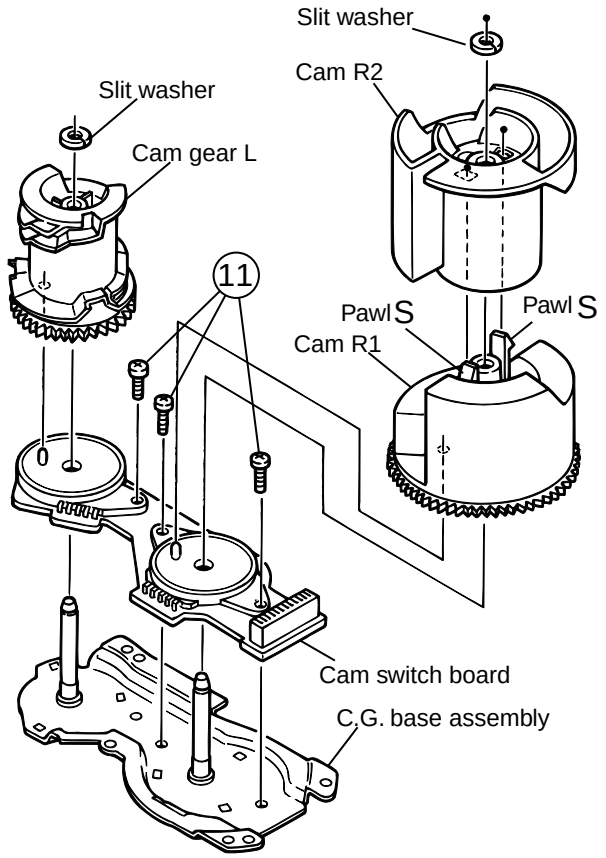


Fig.23

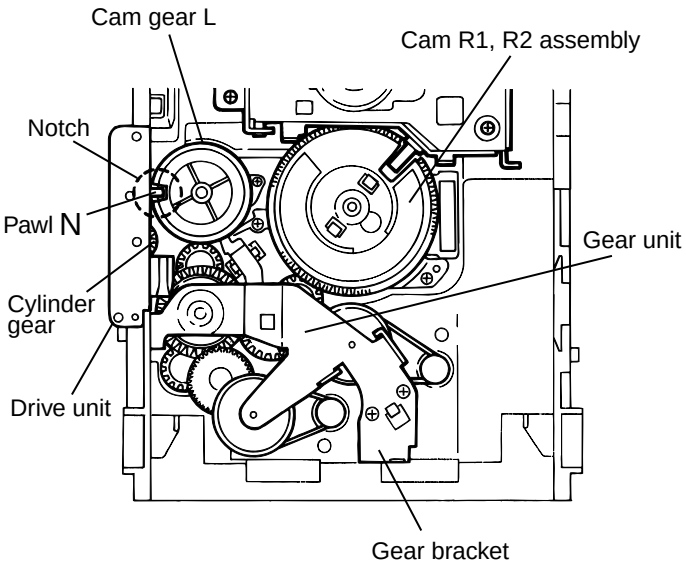


Fig.24

< Cassette Mechanism Section >

■ Removing the Playback,Recording and Eraser Heads (See Fig.1~3)

1. While shifting the trigger arms seen on the right side of the head mount in the arrow direction,turn the flywheel R in counterclockwise direction until the head mount has gone out with a click (See Fig. 1).
2. When the flywheel R is rotated in counterclockwise direction, the playback head will be turned in counterclockwise direction from the position in Fig.2 to that in Fig.3.
3. At this position, disconnect the flexible P.C.board (outgoing from the playback head) from the connector CN301 on the head amp. and mechanism control P.C. board.
4. After dismounting the FPC holder,remove the flexible P.C.board.
5. Remove the flexible P.C.board from the chassis base.
6. Remove the spring "a" from behind the playback head.
7. Loosen the reversing azimuth screw retaining the playback head.
8. Take out the playback head from the front of the head mount.
9. The recording and eraser heads should also be removed similarly according to Steps 1~8 above.

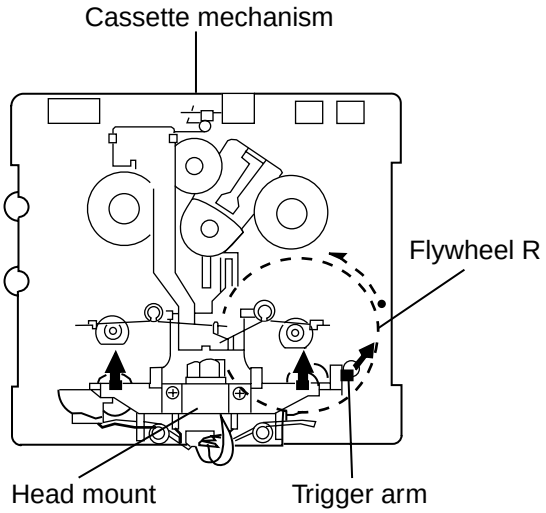


Fig.1 (Mechanism A side)

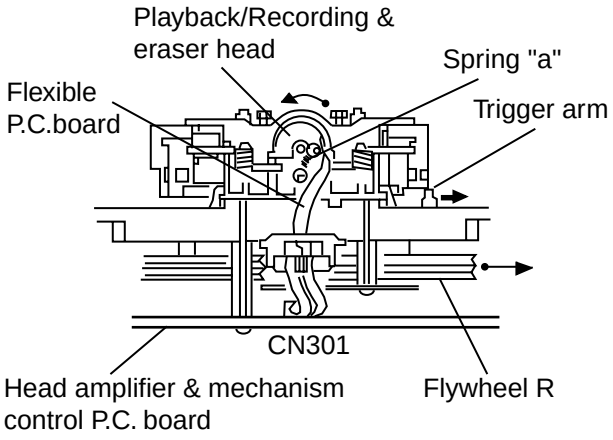


Fig.2 (Mechanism A side)

● Reassembling the Playback, Recording and Eraser Heads (See Fig.2,3)

1. Reassemble the playback head from the front of the head mount to the position as shown in Fig.3.
2. Fix the reversing azimuth screw.
3. Set the spring a from behind the playback head.
4. Attach the flexible P.C.board to the chassis base, and fix it with the FPC holder as shown in Fig.3.
5. The recording and eraser heads should also be reassembled similarly according to Steps 1~4 above.

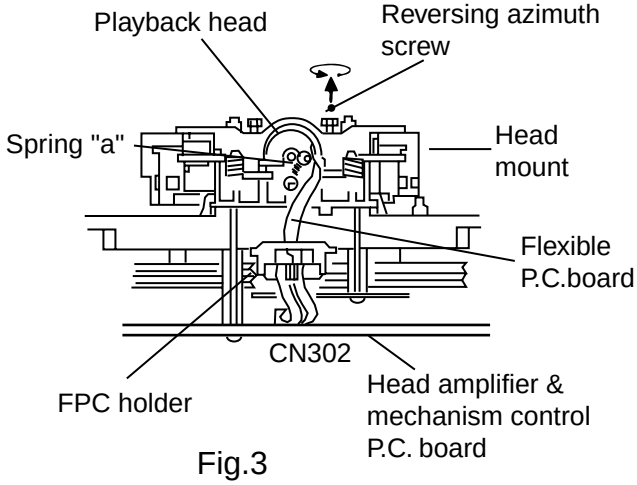


Fig.3 (Mechanism B side)

■ Removing the head Amp.and Mechanism Control P.C.Board (See Fig. 4)

1.Remove the cassette mechanism assembly.
2.After turning over the cassette mechanism assembly,remove the five screws "A" retaining the head amp. and mechanism control P.C. board
3.Disconnect the connectors CN303 and CN304 on the P.C.Board and the connectors CN1 on both the right and left side reel pulse P.C.Boards.
4.When necessary, remove the 4pin parallel wire soldered to the main motor

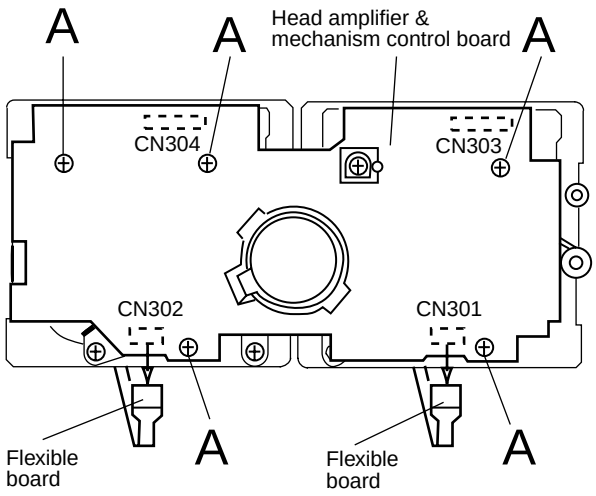


Fig.4

■ Removing the Capstan Motor Assembly

1.Remove the six screws "B" retaining capstan motor assembly (See Fig. 5).
2.While raising the capstan motor, remove the capstan belts A and B respectively from the motor pulley (See Fig. 6).

Caution 1: Be sure to handle the capstan belts so carefully that these belts will not be stained by grease and other foreign matter. Moreover, these belts should be hand while referring to the capstan belt hanging method.

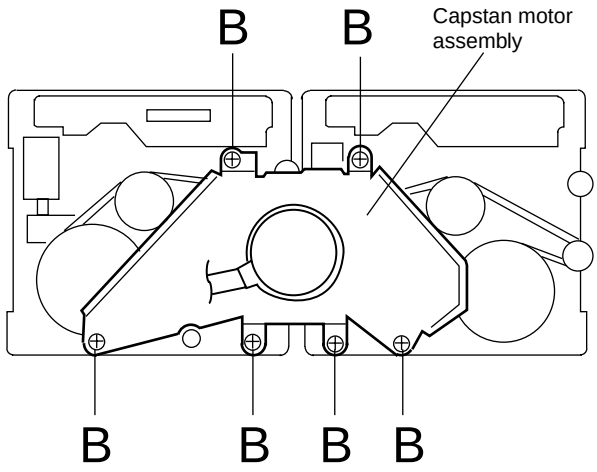


Fig.5

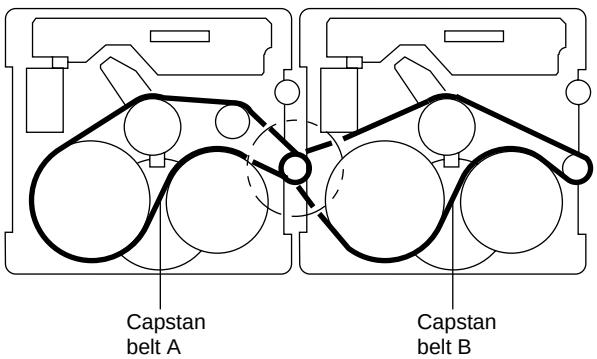


Fig.7

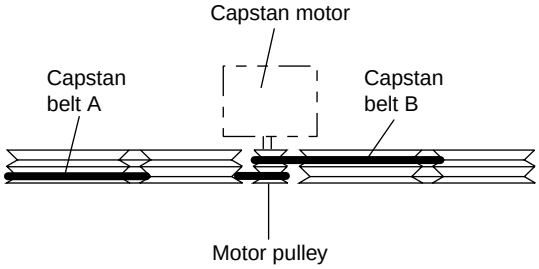


Fig.6

■ Removing the Capstan Motor (See Fig. 8)

From the joint bracket, remove the two screws "C" retaining the capstan motor.

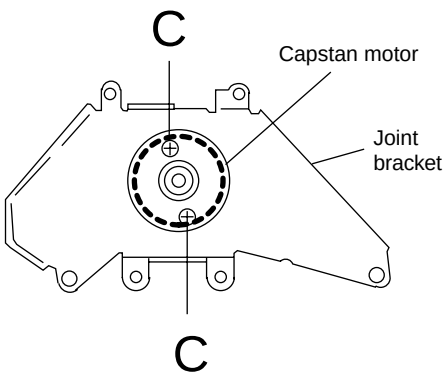


Fig.8

■ Removing the Flywheel (See Fig. 9,10)

1.Remove the head amp. and mechanism control P.C.Board.
2.Remove the capstan motor assembly.
3.After turning over the cassette mechanism, remove the slit washers "a" and "b" fixing the capstan shafts R and L, and pull out the flywheels R and L respectively from behind the cassette mechanism.

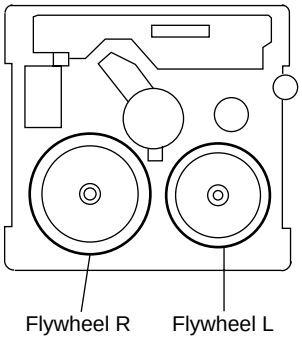


Fig.10

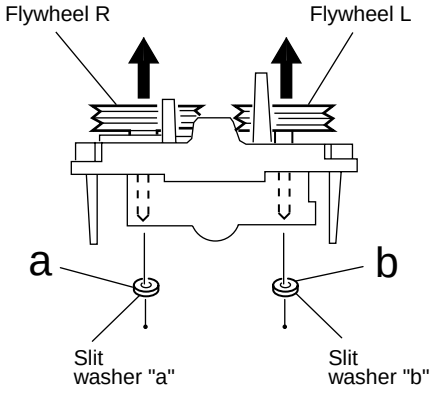


Fig.9

■ Removing the Reel Pulse P.C.Board and Solenoid (See Fig. 11)

1.Remove the five pawls (c,d,e,f,g) retaining the reel pulse P.C.Board.
2.From the surface of the reel pulse P.C.Board parts, remove the two pawls "h" and "i" retaining the solenoid.

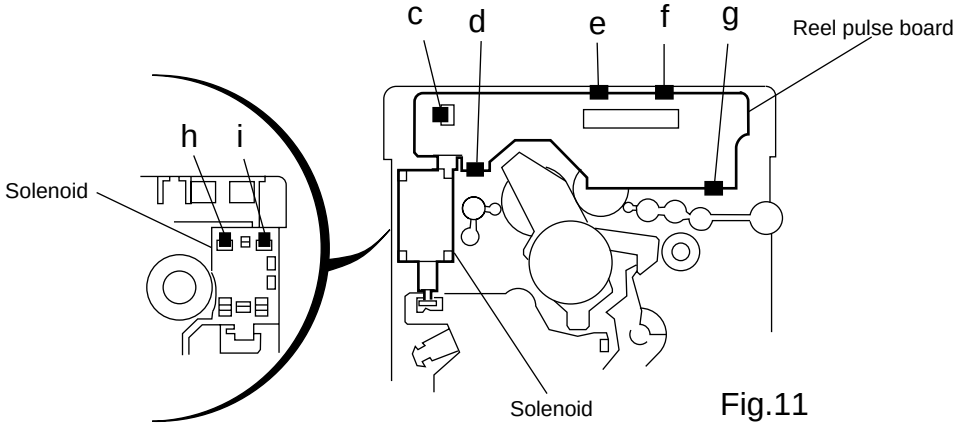


Fig.11

Disassembly method

■ Removing the side cover (See Fig.1)

1. Remove the six screws **A** on the side of the body.

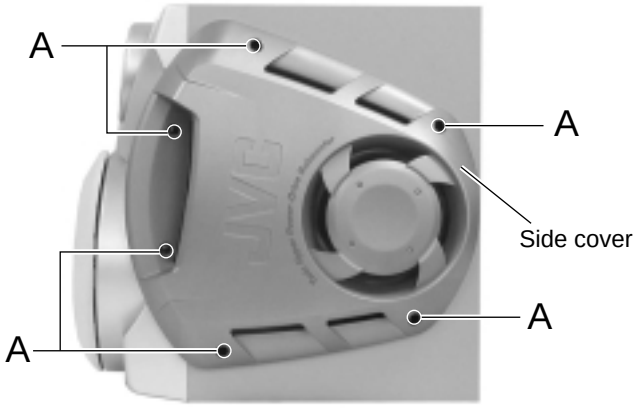


Fig.1

■ Removing the squawker speaker (See Fig.2)

- Prior to performing the following procedure, remove the side cover.

1. Remove the four screws **B** on the side of the body.
2. Disconnect the red and black wires from the speaker terminals on the squawker speaker.

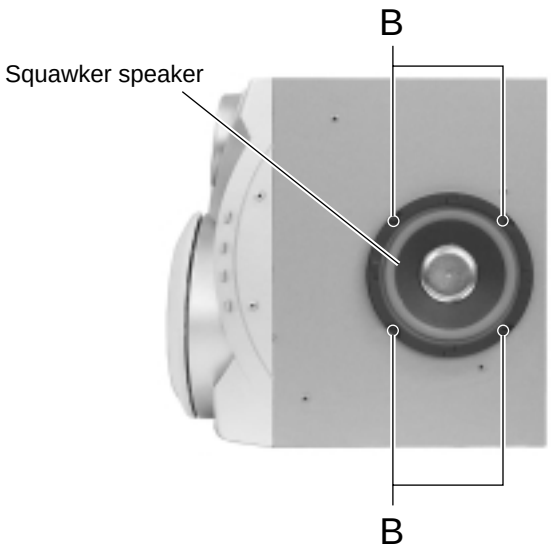


Fig.2

■ Removing the front cover (See Fig.3 to 5)

- Prior to performing the following procedure, remove the side cover.

1. Pull out the saran net toward the front while disengaging the four joints **a**.
2. Remove the two screws **C** and **D** respectively.
3. Remove the front cover toward the front and disconnect the yellow and black wires from the two tweeter speaker terminals.

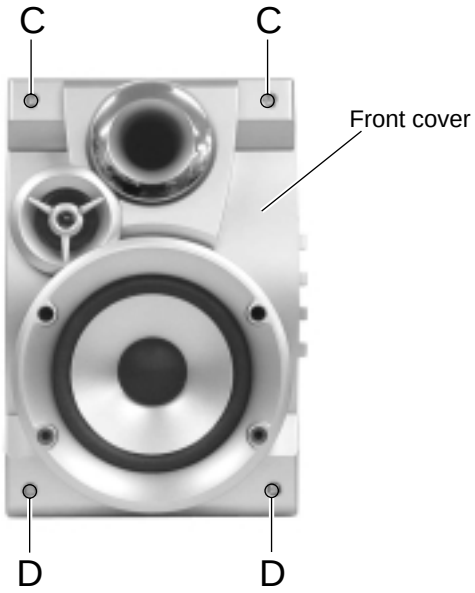


Fig.4

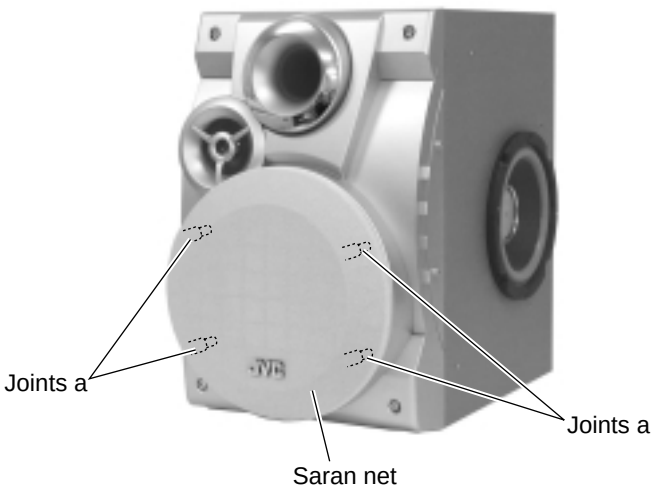


Fig.3

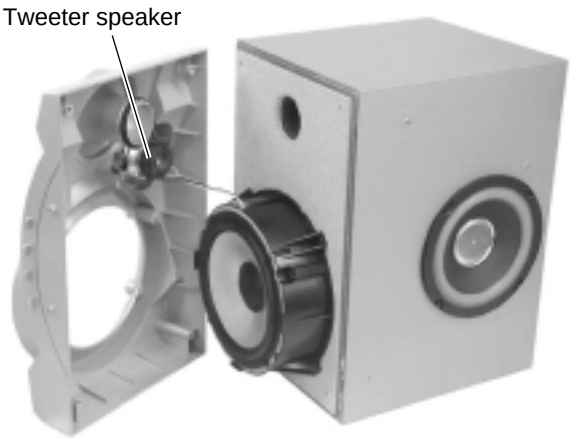


Fig.5

■Removing the woofer speaker (See Fig.6)

・ Prior to performing the following procedure, remove the side cover and the front cover.

1. Remove the four screws **E** on the front of the body.

2. Pull out the woofer speaker toward the front and disconnect the wire (yellow and black,blue and black) from the two speaker terminals.

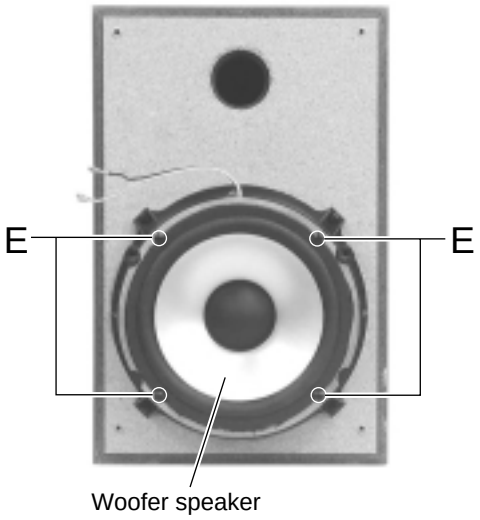


Fig.6

■Removing the tweeter speaker (See Fig.7)

・ Prior to performing the following procedure, remove the side cover and the front cover.

1. Remove the two screws **F** attaching the tweeter speaker on the back of the front cover.

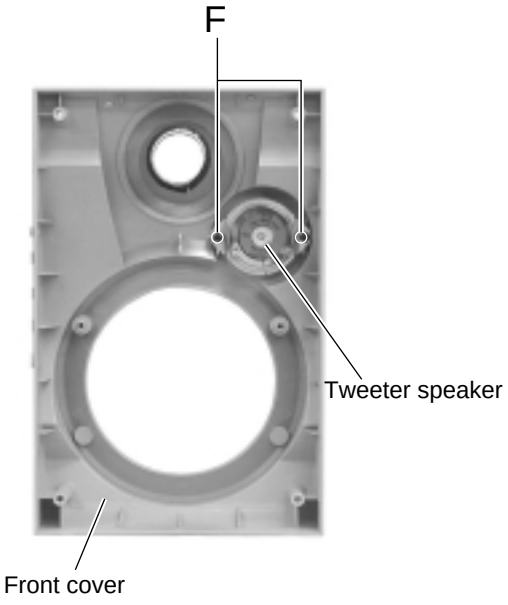


Fig.7

Measurement instruments required for adjustment

1. Low frequency oscillator,
   This oscillator should have a capacity to output 0dBs to 600ohm at an oscillation frequency of 50Hz-20kHz.
2. Attenuator impedance : 600ohm
3. Electronic voltmeter
4. Frequency counter
5. Wow flutter meter
6. Test tape
   VT712 : For Tape speed and wow flutter (3kHz)
   VT724 : For Reference level (1kHz)
   VT703L : For Head angle(10kHz)

   Because of frequency-mixed tape with 63,1k,10k and 14kHz(250nWb/m -24dB).
   Use this tape together with a filter.
7. Blank tape
   TAPE : AC-225
8. Torque gauge : For play and back tension
   Forward ; TW2111A, Reverse ; TW2121A
   Fast Forward and Rewind ; TW2231A
9. Test disc
   : CTS-1000(12cm),GRG-1211(8cm)
10. Jitter meter

Measurement conditions

Power supply voltage
AC120V(60Hz)

Measurement
output terminal : Speaker out
:TP101(Mesuring for TUNER/DECK/CD)
:Dummy load 6ohm

Radio input signal
AM modulation frequency : 400Hz
Modulation factor : 30%
FM modulation frequency : 400Hz
Frequency displacement : 22.5kHz

Frequency Range
A/B/EN
AM 522kHz~1629kHz
FM 87.5MHz~108MHz

US/UJ/UG/UN/UW
AM 531kHz~1602kHz
FM 87.5MHz~108MHz

Standard measurement positions of volume and switch
Power : Standby (Light STANDBY Indicator)
Sub woofer VOL. : Minimum
Sound mode : OFF
Main VOL. : 0 Minimum
Traverse mecha set position : Disc 1
Mic MIX VOL : MAX
ECHO : OFF

Precautions for measurement
1. Apply 30pF and 33kohm to the IF sweeper output side and 0.082 F and 100kohm in series to the sweeper input side.
2. The IF sweeper output level should be made as low as possible within the adjustable range.
3. Since the IF sweeper is a fixed device, there is no need to adjust this sweeper.
4. Since a ceramic oscillator is used, there is no need to perform any MPX adjustment.
5. Since a fixed coil is used, there is no need to adjust the FM tracking.
6. The input and output earth systems are separated. In case of simultaneously measuring the voltage in both of the input and output systems with an electronic voltmeter for two channels, therefore, the earth should be connected particularly.
7. In the case of BTL connection amplifier, the minus terminal of speaker is not for earthing. Therefore, be sure not to connect any other earth terminal to this terminal. This system is of an OTL system.

■ DVD section

TEST MODE FOR DVD a INITIALISE THE DVD UNIT BOARD

a) Insert A/C Power Cord

b) At standby mode press Stop Button and CANCEL/DEMO button.

Wait 4 seconds & for the display of " TEST VERSION REGION " i.e. TEST JC 1

c) Press the 'ENTER' button on remocon. The FL panel will display 'EEPROM'.

Plug out and plug in again the power cord. Repeat the process 1(a) and 1(b) again.

Confirm that the Area Code and Region Code is correctly display as below.

Are Code	FL indicate of Area Code in Test mode	Region Code.
J/C	JC	1
UJ	JC	1
UG/UX	2U	2
US/UN/UP	3U	3
UT	UT	3
UW	4U	4
E/EN/B	E	2
A	A	4
EE	EE	5

Note: Please plug out and plug in the power cord from A/C supply before continue the next test.

Adjustment

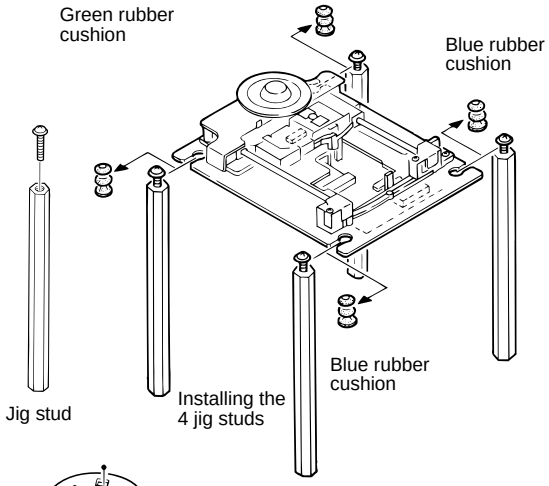
Jig setup

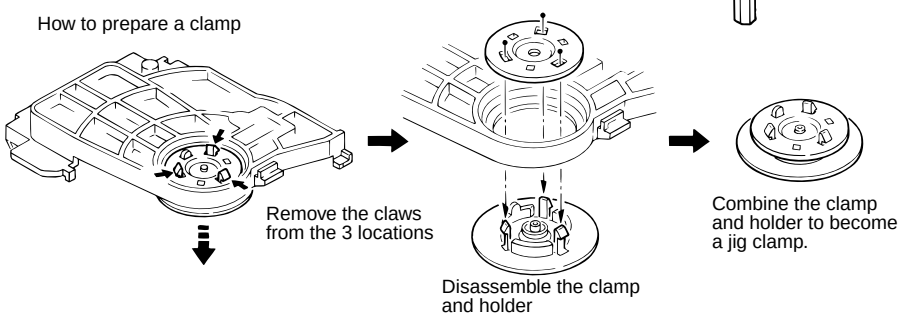
1. Remove the rubber cushion from each of the four corners of the traverse mechanism.
   (When installing be sure not to make a mistake with the cushion colors).
2. Install the jig stud.
3. Make a jig clamp. (Remove the clamp from the set and assemble it as shown in the diagram below.

Note:

How to handle the pickup

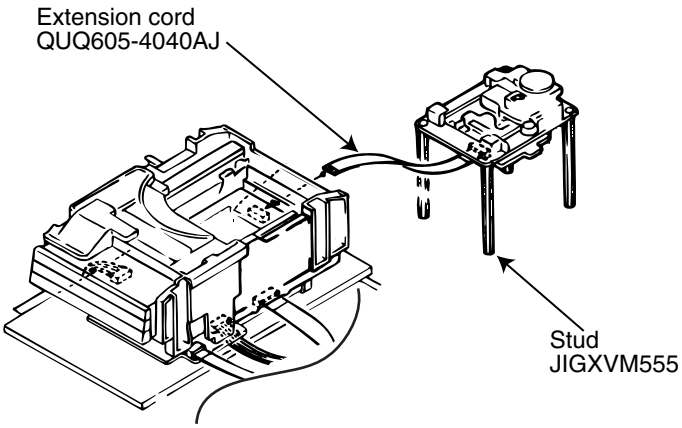
To protect the pickup from electro-static damage, make sure to hold it by the die-cast chassis (optical base). And make sure that pickup lens do not touch the top cover.





Integrated wiring for adjustment

1. Place a board on top of the unit and put the changer on it. Then carry out the wiring of the main unit.
2. Connect a extension cable to the traverse mechanism for adjustment and then connect them to the changer.
3. Remove the solder of the short-circuited flexible wire. Then remove the short-circuited pin from the traverse mechanism
4. Connection is completed.



Adjustment preparation

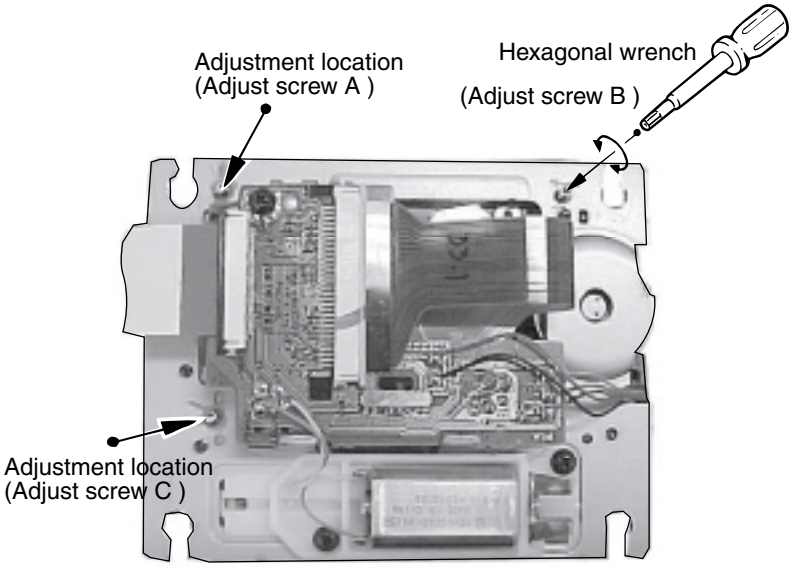
1. The 3 adjustment locations
2. 1.4 mm hexagonal wrench
3. Set the VT-501 or the VT502 test disc.

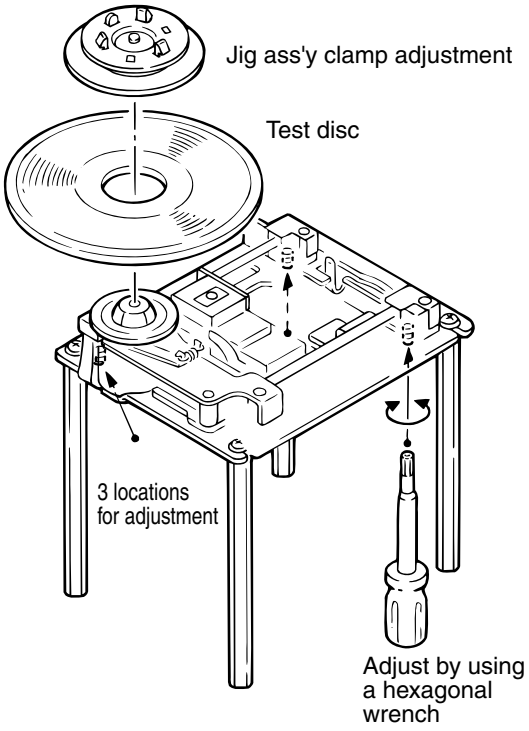
FL jitter display

1. Connect the power cable while pressing the ▲ (OPEN/CLOSE) button of DISC1 and ▷ (PLAY) button simultaneously.
   --- The DISC no. "tEStJ1" is displayed on the FL indicator.
2. Press the 3D-PHONIC key button of remote controller to commence initialization.
3. When the key ▷ (PLAY) is pressed the jitter value is displayed.
4. Adjust the jitter value to minimum by using the adjust screw.

a). Turn the adjustment screw (A and B) clockwise half.
b). Return the adjustment screw (A and B) to former position.
c). Turn the adjustment screw (A and B) counterclockwise half.
d). Set the adjustment screw (A and B) to the position of best jitter at three positions.

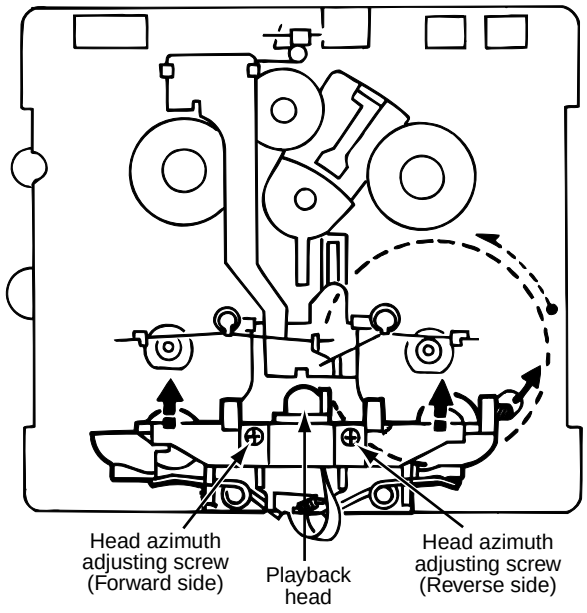
Next, do it similar to the above-mentioned in adjustment screw A and C.



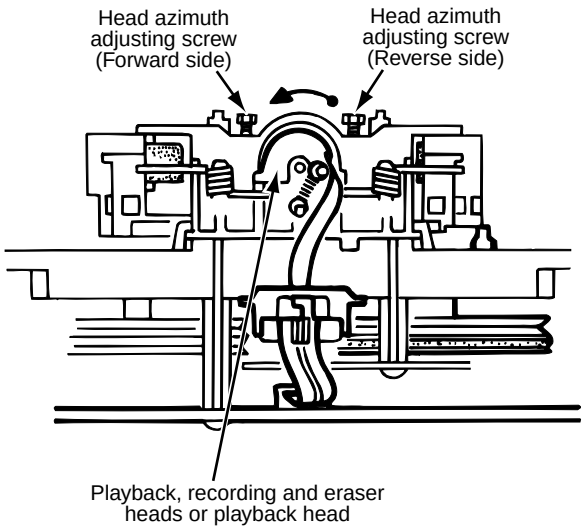


■ Arrangement of adjusting positions

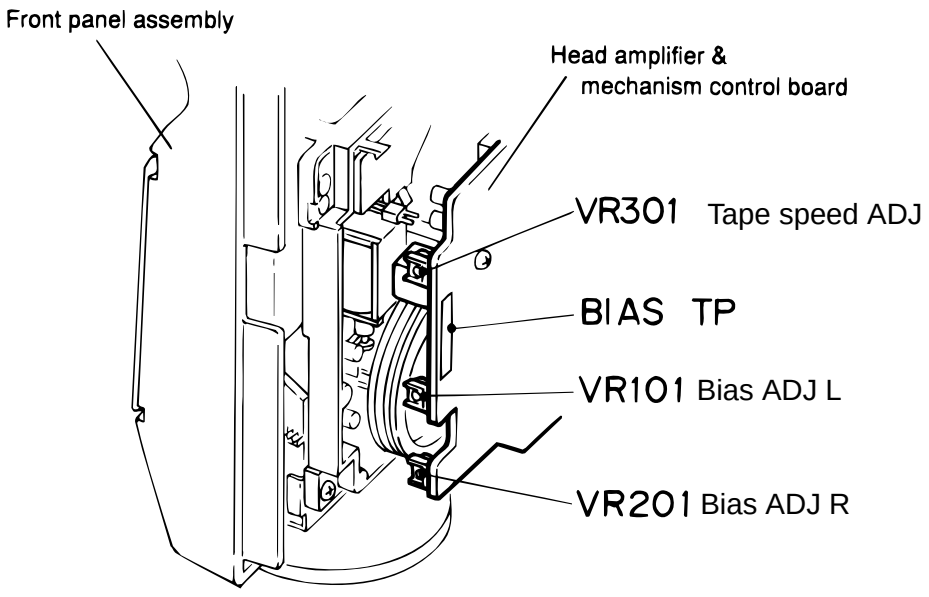
Cassette mechanism section (Mechanism A section)



Cassette mechanism section (Back side)



Cassette Mechanism Unit Section



■ Tape recorder section

Items	Measurement conditions	Measurement method	Standard values	Adjusting positions
Confirmation of head angle	Test tape :VT703L(10kHz) Measurement output terminal :Speaker terminal Speaker R (Load resistor:6Ω) :Headphone terminal	1.Playback the test tape VT703L(10kHz). 2.With the playback mechanism or recording & playback mechanism, adjust the head azimuth screw so that the forward and reverse output levels become maximum.After adjustment,lock the head azimuth at least by half a turn. 3.In either case,this adjustment should be performed in both the forward and reverse directions with the head azimuth screw.	Maximum output	Adjust the head azimuth screw only when the head has been changed.
Confirmation of tape speed	Test tape :VT712(3kHz) Measurement output terminal :Headphone terminal	<Constant speed> Adjust VR301 so that the frequency counter reading becomes 3,000Hz±60Hz when playing back the test tape VT712(3kHz)with the playback mechanism or playback and recording mechanism after ending forward winding of the tape.	Tape speed of decks (A and B) :3,000Hz ±60Hz	VR301

■ Reference values for confirmation items

Items	Measurement conditions	Measurement method	Standard values	Adjusting positions
Double tape speed	Test tape :VT703L(10kHz) Measurement output terminal :Speaker terminal Speaker R (Load resistance:6Ω) measurement output terminal :Headphone terminal	After setting to the double speed motor, confirm that the frequency counter reading becomes 4,800+400/-300Hz when the test tape VT712 (3kHz) has been play back with the playback mechanism.	4,800+400/ -300Hz	Playback mechanism side
Difference between the forward and reverse speed. P.mecha and R/P mecha speed		When the test tape VT712(3kHz) has been played back with the playback mechanism or recording and playback mechanism at the beginning of forward winding, the frequency counter reading of the difference between both of the mechanisms should be 6.0Hz or less.	60Hz or less	Both the playback and recording & playback mechanism
Wow & flutter	Test tape :VT712(3kHz) Measurement output terminal :Headphone terminal	When the test tape VT712(3kHz) has been played back with the playback mechanism or recording and playback mechanism at the beginning of forward winding the frequency counter reading of wow & flutter should be 0.25% or less(WRMS).	with in 0.25% JIS(WTD)	Both the playback and recording & playback mechanism

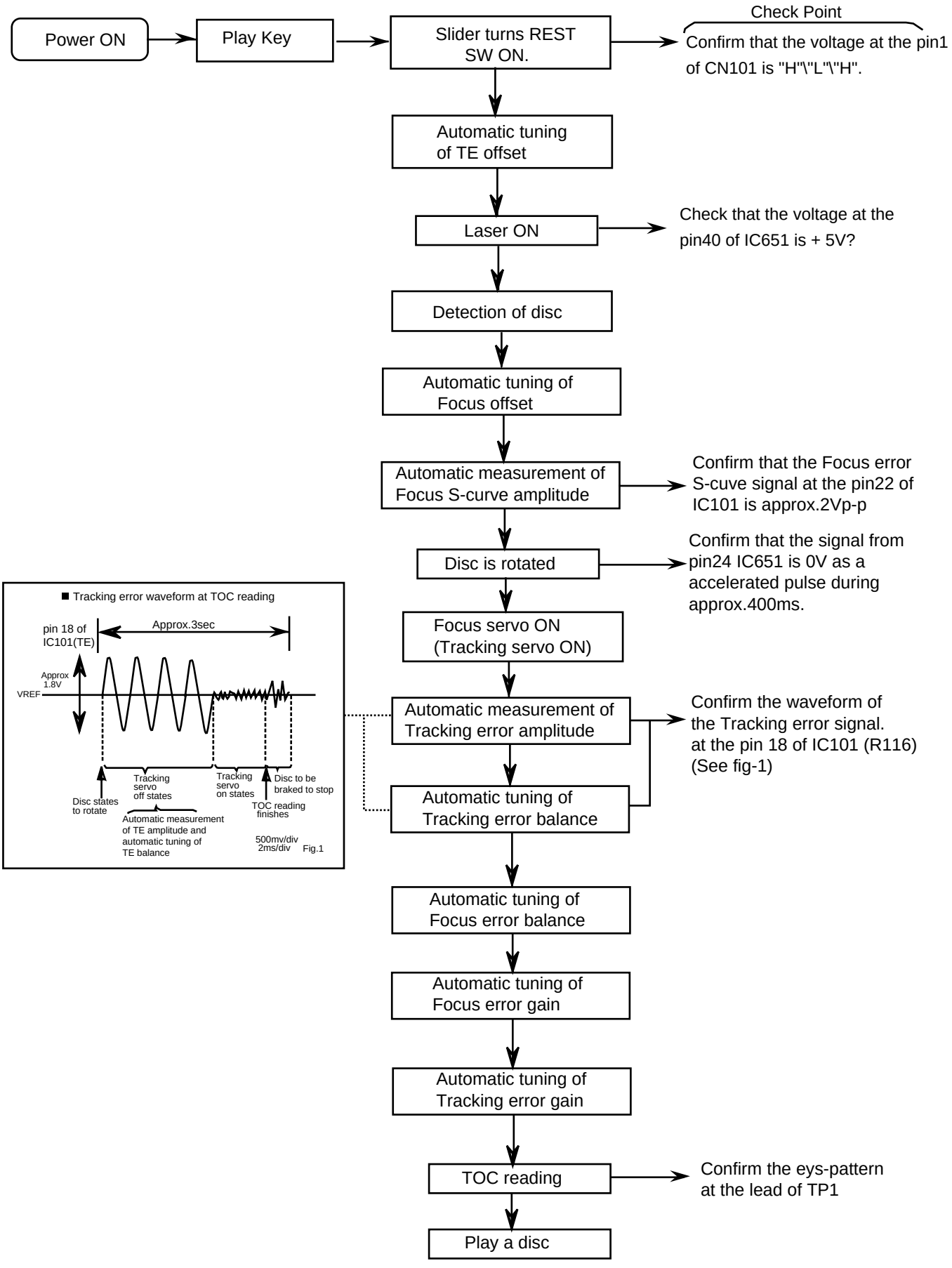
■ Electrical performance

Items	Measurement conditions	Measurement method	Standard values	Adjusting positions
Adjustment of recording bias current (Reference value)	*Mode : Forward or reverse mode *Recording mode *Test tape : AC-225 Measurement output terminal :Both recording and headphone terminals	1.With the recording and playback mechanism, load the test tapes(AC-225 to TYP Ⅰ),and set the mechanism to the recording and pausing conditions in advance. 2.After connecting 100Ω in series to the recorder head,measure the bias current with a valve voltmeter at both of the terminals. 3.After resetting the [PAUSE] mode,start recording. At this time,adjust VR101 for LcH and VR201 for RcH so that the recording bias current values become 4.0μA (TYP Ⅰ).	AC-225 :4.20μA	LcH :VR101 RcH :VR201
Adjustment of recording and playback frequency characteristics	Reference frequency :1kHz and 10kHz (REF:-20dB) Test tape :TYP Ⅰ AC-225 Measurement input terminal :OSC IN	1.With the recording and playback mechanism,load the test tape(AC-225 to TYP Ⅰ),and set the mechanism to the recording and pausing condition in advance. 2.While repetitively inputting the reference frequency signal of 1kHz and 10kHz from OSC IN, record and playback the test tape. 3.While recording and playing back the test tape in TYP Ⅰ,adjust VR101 for LcH and VR201 for RcH so that the output deviation between 1kHz and 10kHz becomes -1dB±2dB.	Output deviation between 1kHz and 10kH :-1dB±2dB	LcH :VR101 RcH :VR201

■ Reference values for electrical function confirmation items

Items	Measurement conditions	Measurement method	Standard values	Adjusting positions
Recording bias frequency	*Recording and playback side forward or reverse *Test tape :TYP Ⅰ AC-225 *Measurement terminal BIAS TP on P.C.board	1.While changing over to and from BIAS 1 and 2, confirm that the frequency is changed. 2.With the recording and playback mechanism. load the test tape (AC-225 to TYP Ⅰ),and set the mechanism to the recording and pausing conditions in advance. 3.Confirm that the BIAS TP frequency on the P.C.board is 100kHz±6kHz.	100kHz +9kHz -7kHz	
Eraser current (Reference value)	*Recording and playback side forward or reverse *Recording mode *Test tape :AC-225 Measurement terminal Both of the eraser head	1.With the recording and playback mechanism, load the test tapes(AC-225 to TYP Ⅰ),and set the mechanism to the recording and pausing condition in advance. 2.After setting to the recording conditions,connect 1MΩ in series to the eraser head on the recording and playback mechanism side,and measure the eraser current from both of the eraser terminal.	TYP Ⅰ :75mA	

Flow of functional operation until TOC read

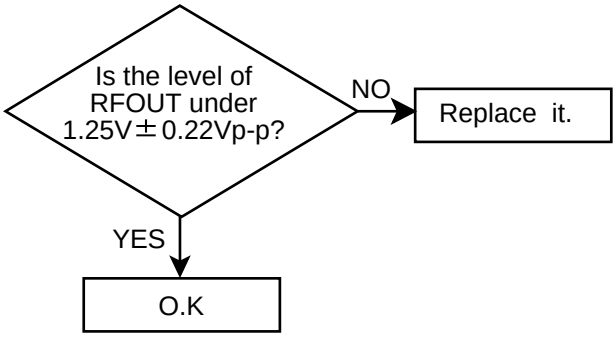


Maintenance of laser pickup

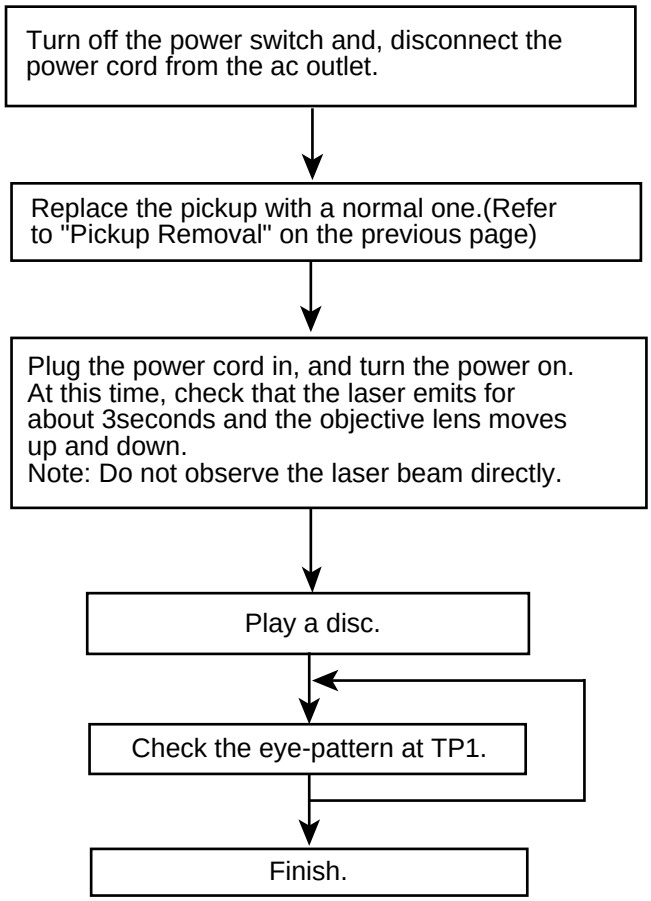
(1) Cleaning the pick up lens
Before you replace the pick up, please try to clean the lens with a alcohol soaked cotton swab.

(2) Life of the laser diode
When the life of the laser diode has expired, the following symptoms will appear.

1. The level of RF output (EFM output : amplitude of eye pattern) will below.



Replacement of laser pickup

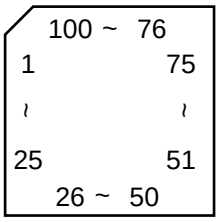


(3) Semi-fixed resistor on the APC PC board
The semi-fixed resistor on the APC printed circuit board which is attached to the pickup is used to adjust the laser power. Since this adjustment should be performed to match the characteristics of the whole optical block, do not touch the semi-fixed resistor.
If the laser power is lower than the specified value, the laser diode is almost worn out, and the laser pickup should be replaced.
If the semi-fixed resistor is adjusted while the pickup is functioning normally, the laser pickup may be damaged due to excessive current.

Description of major ICs

■ MN102L62GEJ (IC401) : Unit CPU

1.Terminal layout

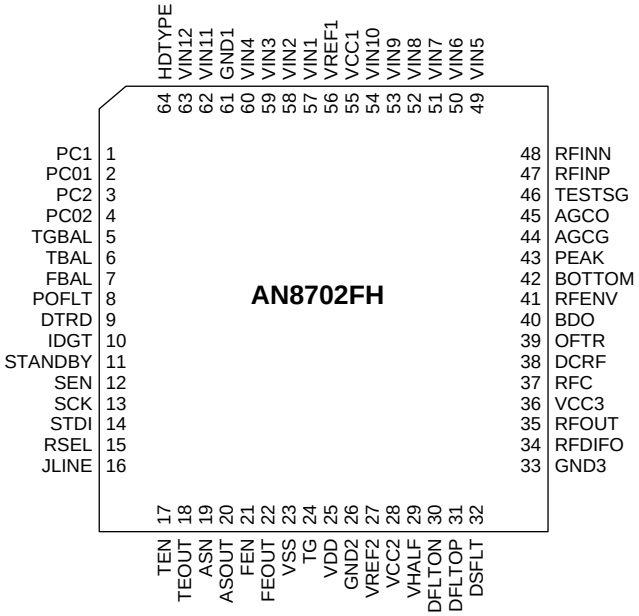


2.Pin function

Pin No.	Symbol	I/O	Function	Pin No.	Symbol	I/O	Function
1	WAIT	I	Micon wait signal input	51	FGIN		
2	RE	O	Read enable	52	TRS		
3	SPMUTE	O	Spindle muting output to IC251	53	ADSCEN	O	Serial enable signal for ADSC
4	WEN	O	Write enable	54	VDD	-	Power supply
5	CS0	-	Non connect	55	FEPEN	O	Serial enable signal for FEP
6	CS1	O	Chip select for ODC	56	SLEEP	O	Standby signal for FEP
7	CS2	O	Chip select for ZIVA	57	BUSY	I	Communication busy
8	CS3	O	Chip select for outer ROM	58	REQ	O	Communication Request
9	DRVMUTE	O	Driver mute	59	CIRCEN	O	CIRC command select
10	SPKICK	O	Spin kick (Non connect)	60	HSSEEK	-	Non connect
11	LSIRST	O	LSI reset	61	VSS	-	Ground
12	WORD	O	Bus selection input	62	EPCS	O	EEPROM chip select
13	A0	O	Address bus 0 for CPU	63	EPSK	O	EEPROM clock
14	A1	O	Address bus 1 for CPU	64	DPDI	I	EEPROM data input
15	A2	O	Address bus 2 for CPU	65	EPDO	O	EEPROM data output
16	A3	O	Address bus 3 for CPU	66	VDD	-	Power supply
17	VDD	-	Power supply	67	SCLKO	I	Communication clock
18	SYSCLK	O	System clock signal output	68	S2UDT	I	Communication input data
19	VSS	-	Ground	69	U2SDT	O	Communication output data
20	XI	-	Not use (Connect to vss)	70	CPSCK	O	Clock for ADSC serial
21	XO	-	Non connect	71	SDIN	I	ADSC serial data input
22	VDD	-	Power supply	72	SDOUT	O	ADSC serial data output
23	OSCI	I	Clock signal input(13.5MHz)	73	-	-	Not use
24	OSCO	O	Clock signal output(13.5MHz)	74	-	-	Not use
25	MODE	I	CPU Mode selection input	75	NMI	-	Not use
26	A4	O	Address bus 4 for CPU	76	ADSCIRQ	I	Interrupt input of ADSC
27	A5	O	Address bus 5 for CPU	77	ODCIRQ	I	Interrupt input of ODC
28	A6	O	Address bus 6 for CPU	78	DECIRQ	I	Interrupt input of ZIVA
29	A7	O	Address bus 7 for CPU	79	WAKEUP	O	Not use
30	A8	O	Address bus 8 for CPU	80	ODCIRQ2	I	Interruption of system control
31	A9	O	Address bus 9 for CPU	81	ADSEP	I	Address data selection input
32	A10	O	Address bus 10 for CPU	82	RST	I	Reset input
33	A11	O	Address bus 11 for CPU	83	VDD	-	Power supply
34	VDD	-	Power supply	84	TEST1	I	Test signal 1 input
35	A12	O	Address bus 12 for CPU	85	TEST2	I	Test signal 2 input
36	A13	O	Address bus 13 for CPU	86	TEST3	I	Test signal 3 input
37	A14	O	Address bus 14 for CPU	87	TEST4	I	Test signal 4 input
38	A15	O	Address bus 15 for CPU	88	TEST5	I	Test signal 5 input
39	A16	O	Address bus 16 for CPU	89	TEST6	I	Test signal 6 input
40	A17	O	Address bus 17 for CPU	90	TEST7	I	Test signal 7 input
41	A18	O	Address bus 18 for CPU	91	TEST8	I	Test signal 8 input
42	A19	O	Address bus 19 for CPU	92	VSS	-	Ground
43	VSS	-	Ground	93	D0	I/O	Data bus 0 of CPU
44	A20	O	Address bus 20 for CPU	94	D1	I/O	Data bus 1 of CPU
45	TXSEL	O	TX Select	95	D2	I/O	Data bus 2 of CPU
46	HAGUP	O		96	D3	I/O	Data bus 3 of CPU
47	CD/DVD	O	Foucs balance & leaser power select	97	D4	I/O	Data bus 4 of CPU
48	ADPD	O	Power up out put	98	D5	I/O	Data bus 5 of CPU
49	HMFON	O		99	D6	I/O	Data bus 6 of CPU
50	TRVSW	I	Detection switch of traverse inside	100	D7	I/O	Data bus 7 of CPU

■ AN8702FH (IC101) : Frontend processor

1.Terminal layout

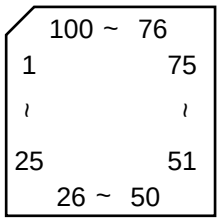


2.Pin function

Pin No.	Symbol	I/O	Description	Pin No.	Symbol	I/O	Description
1	PC1	I	Input for Laser current monitor	34	RFDIFO	O	RF operation output terminal
2	PC01	O	Laser power control output for DVD	35	RFOUT	O	RF output terminal
3	PC2	I	Photo detector fo CD	36	VCC3	-	Power supply terminal 5V
4	PC02	O	Laser power control output for CD	37	RFC	I	Filter for RF amplifier
5	TGBAL	I	Tangential phase balance control terminal	38	DCRF	O	All addition amplifier capacitor terminal
6	TBAL	I	Tracking balance control terminal	39	OFTR	O	OFTR output terminal
7	FBAL	I	Focus balance control terminal	40	BDO	O	BDO output terminal
8	POFLT	O	Track detection threshold level terminal	41	RFENV	O	RF envelope output terminal
9	DTRD	I	Data slice part data read signal input terminal (For RAM)	42	BOTTOM	O	Bottom envelope detection filter terminal
				43	PEAK	O	Peak envelope detection filter terminal
10	IDGT	I	Data slice part address part gate signal input terminal(For RAM)	44	AGCG	O	AGC amplifier gain control terminal
				45	AGCO	O	AGC amplifier level control terminal
11	STANDBY	I	Standby mode control terminal	46	TESTSG	I	TEST signal input terminal
12	SEN	I	SEN(Serial data input terminal)	47	RFINP	I	RF signal positive input terminal
13	SCK	I	SCK(Serial data input terminal)	48	RFINN	I	RF signal negative input terminal
14	STDI	I	STDI(Serial data input terminal)	49	VIN5	I	RF input of external division into 4 terminal for CD
15	RSEL	I	DVD and CD selection	50	VIN6	I	RF input of external division into 4 terminal for CD
16	JLINE	I	J-line setting output (FEP)	51	VIN7	I	RF input of external division into 4 terminal for CD
17	TEN	I	Tracking error output amplifier reversing input terminal	52	VIN8	I	RF input of external division into 4 terminal for CD
18	TEOUT	O	Tracking error signal output terminal	53	VIN9	I	RF input of external division into 2 terminal for DVD
19	ASN	I	Off set adjustment terminal for DRC	54	VIN10	I	RF input of external division into 2 terminal for DVD
20	ASOUT	O	All added signal output terminal	55	VCC1	-	Power supply terminal 5V
21	FEN	I	Focus error output amplifier reversing input terminal	56	VREF1	O	VREF1 voltage output terminal
22	FEOUT	O	Focus error signal output terminal	57	VIN1	I	External division into four (DVD/CD) RF input terminal1
23	VSS	-	Connect to GND				
24	TG	O	Tangential phase error signal output terminal	58	VIN2	I	External division into four (DVD/CD) RF input terminal2
25	VDD	-	Power supply terminal 3V				
26	GND2	-	Connect to GND	59	VIN3	I	External division into four (DVD/CD) RF input terminal3
27	VREF2	O	VREF2 voltage output terminal				
28	VCC2	-	Power supply terminal 5V	60	VIN4	I	External division into four (DVD/CD) RF input terminal4
29	VHALF	O	VHALF voltage output terminal				
30	DFLTON	O	Filter amplifier reversing output terminal	61	GND1	-	Connect to GND
31	DFLTOP	O	Filter amplifier output terminal	62	VIN11	I	3 beem sub input terminal for CD
32	DSFLT	O	Connected capacitor terminal for filter output	63	VIN12	I	3 beem sub input terminal for CD
33	GND3	-	Connect to GND	64	HDTYPE	I	HD type switching

■ MN101C35DEG (IC810) : System control & FL driver

1.Terminal layout



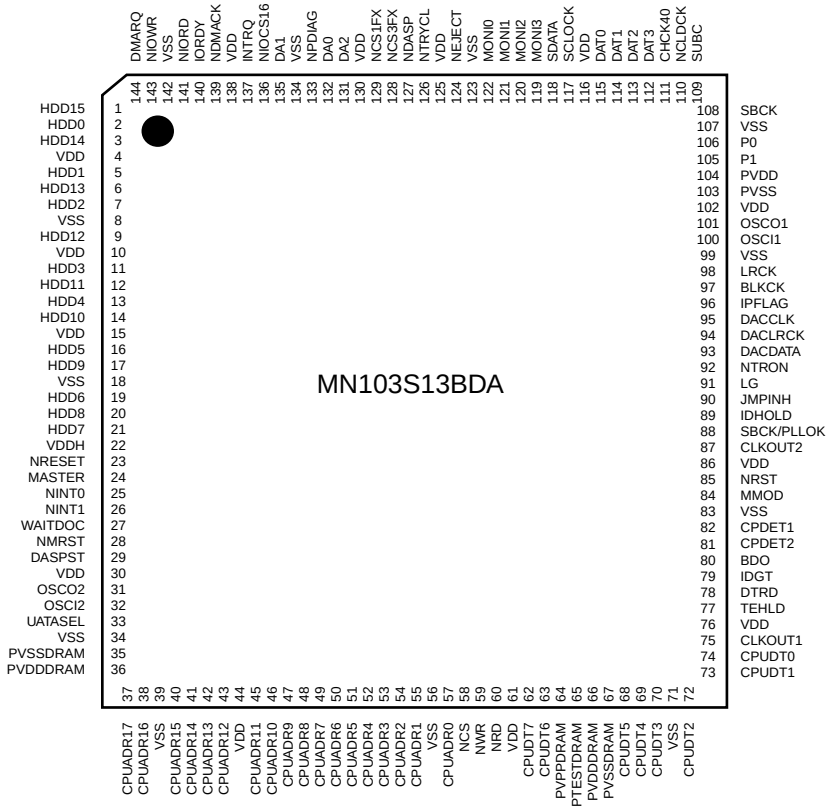
2.Pin function

Pin No.	Symbol	I/O	Function
1	SYSOUT	I	DVD signal output
2	SYSIN	O	DVD signal input
3	DVDCLK	I	DVD signal clock
4	DATAOUT	O	Tuner signal output
5	DATAIN	I	Tuner signal input
6	TUCLK	I	Tuner signal clock
7	DVDCS	I	DVD signal data input
8	VDD	-	Power supply
9	OSC2	I	External terminal for main clock
10	OSC1	O	External terminal for main clock
11	VSS	-	Connect to GND
12	X1	-	Connect to GND
13	NC	-	No connect
14	MMOD	-	Connect to GND
15	VDRF-	-	Connect to GND
16	KEY1	I	Key input terminal 1
17	KEY2	I	Key input terminal 2
18	KEY3	I	Key input terminal 3
19	KEY4	I	Key input terminal 4
20	SLCKEY1	I	SLC key input 1
21	SLCKEY2	I	SLC key input 2
22	H/P-IN	O	Head phone signal output
23	SPIDTI	I	FL level data input
24	VREF+	I	Reference voltage terminal
25	SMODE+	I	Surround volume control input
26	RST	I	Reset input
27	BASSVOL+	O	E.volume control signal output +
28	BASSVOL-	O	E.volume control signal output -
29	ECHO2	O	Echo switching control 2
30	RDSDATA /ECHO1	O	Echo switching control 1
31	SPIA	O	FL level control signal A
32	SPIB	O	FL level control signal B
33	REMAIN	I	Remote control signal input
34	PHOTOA	I	Reel pulse detection A
35	PHOTOB	I	Reel pulse detection B
36	DVDHBSY	O	DVD signal input
37	RDSCLK	O	Serial clock switching for RDS and Echo 2
38	PRT	I	Power amplifier output protect detection
39	VOL1CE	O	E.volume data chip enable
40	VSCE	O	System bus chip enable
41	POUT	O	Power ON control output
42	FVOLDA	O	E.volume control data output
43	VOLCK	O	E.volume data communication clock

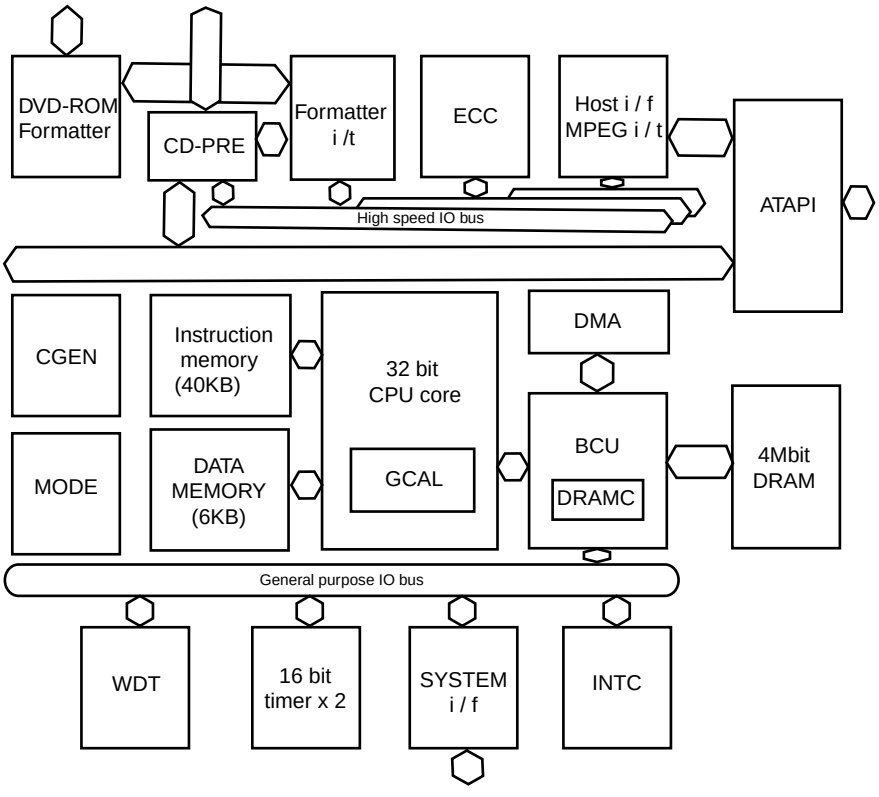
Pin No.	Symbol	I/O	Function
44	EXIT1	O	Chip enable for EXT.IC
45	SLCCE	O	Chip enable for SLC control
46	DVDRST	O	DVD reset
47	G17	O	FL drive control
48	G16	O	FL drive control
49	G15	O	FL drive control
50	G14	O	FL drive control
51	G13	O	FL drive control
52	G12	O	FL drive control
53	G11	O	FL drive control
54	G10	O	FL drive control
55	G9	O	FL drive control
56	G8	O	FL drive control
57	G7	O	FL drive control
58	G6	O	FL drive control
59	G5	O	FL drive control
60	G4	O	FL drive control
61	G3	O	FL drive control
62	G2	O	FL drive control
63	G1	O	FL drive control
64	P22	O	FL drive control
65	P21	O	FL drive control
66	P20	O	FL drive control
67	P19	O	FL drive control
68	P18	O	FL drive control
69	P17	O	FL drive control
70	P16	O	FL drive control
71	P15	O	FL drive control
72	P14	O	FL drive control
73	P13	O	FL drive control
74	P12	O	FL drive control
75	P11	O	FL drive control
76	P10	O	FL drive control
77	P9	O	FL drive control
78	P8	O	FL drive control
79	P7	O	FL drive control
80	P6	O	FL drive control
81	P5	O	FL drive control
82	P4	O	FL drive control
83	P3	O	FL drive control
84	P2	O	FL drive control
85	P1	O	FL drive control
86	TUCE	O	Tuner control chip enable
87	VOL2CE	O	Volume control chip enable
88	VSCLK	O	Volume clock
89	DVD1LED	O	Disc 1 LED drive
90	DVD2LED	O	Disc 2 LED drive
91	DVD3LED	O	Disc 3 LED drive
92	R_SEARCH	I	Tuner signal detection
93	MSI	I	Detection between the broadcasting
94	MPX	I	Stereo signal detection
95	INH	O	Tuner signal inhibit
96	F_SEARCH		Tuner signal detection
97	VOL-		Volume drive control
98	VOL+		Volume drive control
99	SMODE-	O	Sub woofer volume control
100	VPP	I	Power supply

■ MN103S13BDA (IC301) : Optical disc controller

1.Terminal layout



2.Block diagram



3.Pin function (1/3)

Pin No.	Symbol	I/O	Description
1	HDD15	I/O	ATAPI Data
2	HDD0	I/O	ATAPI Data
3	HDD14	I/O	ATAPI Data
4	VDD	-	Power supply 3V
5	HDD1	I/O	ATAPI Data
6	HDD13	I/O	ATAPI Data
7	HDD2	I/O	ATAPI Data
8	VSS	-	Connect to GND
9	HDD12	I/O	ATAPI Data
10	VDD	-	Power supply 2.7V
11	HDD3	I/O	ATAPI Data
12	HDD11	I/O	ATAPI Data
13	HDD4	I/O	ATAPI Data
14	HDD10	I/O	ATAPI Data
15	VDD	-	Power supply 3V
16	HDD5	I/O	ATAPI Data
17	HDD9	I/O	ATAPI Data
18	VSS	-	Connect to GND
19	HDD6	I/O	ATAPI Data
20	HDD8	I/O	ATAPI Data
21	HDD7	I/O	ATAPI Data
22	VDDH		
23	NRESET	I	ATAPI Reset input
24	MASTER	I/O	ATAPI Master/slave select
25	NINT0	O	Interruption of system control 0
26	NINT1	O	Interruption of system control 1
27	WAITDOC	O	Wait control of system control
28	NMRST	O	Reset of system control (Connect to TP302)
29	DASPST	I	Setting of initial value of DASP signal
30	VDD	-	Power supply 3V
31	OSCO2	O	Non connect
32	OSCI2	I	Non connect
33	UATASEL	I	Connect to VSS
34	VSS	-	Connect to GND
35	PVSSDRAM		Connect to VSS
36	PVDDDRAM		Connect to VDD(2.7V)
37	CPUADR17	I	System control address
38	CPUADR16	I	System control address
39	VSS	-	Connect to GND
40	CPUADR15	I	System control address
41	CPUADR14	I	System control address
42	CPUADR13	I	System control address
43	CPUADR12	I	System control address
44	VDD	-	Power supply 2.7V
45	CPUADR11	I	System control address
46	CPUADR10	I	System control address
47	CPUADR9	I	System control address
48	CPUADR8	I	System control address
49	CPUADR7	I	System control address
50	CPUADR6	I	System control address

3.Pin function (2/3)

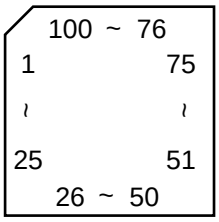
Pin No.	Symbol	I/O	Description
51	CPUADR5	I	System control address
52	CPUADR4	I	System control address
53	CPUADR3	I	System control address
54	CPUADR2	I	System control address
55	CPUADR1	I	System control address
56	VSS	-	Connect to GND
57	CPUADR0	I	System control address
58	NCS	I	System control chip select
59	NWR	I	Writing system control
60	NRD	I	Reading system control
61	VDD	-	Power supply 3V
62	CPUDT7	I/O	System control data
63	CPUDT6	I/O	System control data
64	PVPPDRAM	O	Connect to VSS
65	PTESTDRAM	I	Connect to VSS
66	PVDDDRAM		Connect to VDD(2.7V)
67	PVSSDRAM		Connect to VSS
68	CPUDT5	I/O	System control data
69	CPUDT4	I/O	System control data
70	CPUDT3	I/O	System control data
71	VSS	-	Connect to GND
72	CPUDT2	I/O	System control data
73	CPUDT1	I/O	System control data
74	CPUDT0	I/O	System control data
75	CLKOUT1	O	Clock signal output (16.9/11.2/8.45MHz)
76	VDD	-	Power supply 3V
77	TEHLD	O	Mirror gate (Connect to TP141)
78	DTRD	O	Data frequency control switch (Connect to TP304)
79	IDGT	O	CAPA switch
80	BDO	I	RF Dropout/BCA data
81	CPDET2	I	Outer capacity detection
82	CPDET1	I	Inner capacity detection
83	VSS	-	Connect to GND
84	MMOD	I	Connect to VSS
85	NRST	I	System reset
86	VDD	-	Power supply 3V
87	CLKOUT2	O	Clock 16.9MHz
88	SBCK/PLLOK	O	Flame mark detection
89	IDOHOLD	O	ID gate for tracking holding
90	JMPINH	O	Jump prohibition
91	LG	O	Land/group switch
92	NTRON	I	Tracking ON
93	DACDATA	O	Serial data output (Connect to TP148)
94	DACLRCK	O	Identification signal of L and R (Connect to TP149)
95	DACCLK	I	Clock for serial data output
96	IPFLAG	I	Input of IP flag
97	BLKCK	I	Sub code/block/input clock
98	LRCK	I	Identification signal of L and R (Connect to VSS)
99	VSS	-	Connect to GND
100	OSCI1	I	Oscillation input terminal 16.9MHz

3.Pin function (3/3)

Pin No.	Symbol	I/O	Description
101	OSCO1	O	Oscillation output terminal 16.9MHz
102	VDD	-	Power supply 3V
103	PVSS	-	Connect to GND
104	PVDD	-	Power supply 3V
105	P1	I/O	Terminal master polarity switch input
106	P0	I/O	CIRC-RAM,OVER/UNDER Interruption
107	VSS	-	Connect to GND
108	SBCK	O	Clock output for sub code,serial input
109	SUBC	I	Sub code,serial input
110	NCLDCK	I	Sub code,flame clock input
111	CHCK40	I	Clock is read to DAT3~0 (Output of division frequency from ADSC)
112	DAT3	I	Data is read from disc (Going side by side output from ADSC)
113	DAT2	I	Data is read from disc (Going side by side output from ADSC)
114	DAT1	I	Data is read from disc (Going side by side output from ADSC)
115	DAT0	I	Data is read from disc (Going side by side output from ADSC)
116	VDD	-	Power supply 3V
117	SCLOCK	I/O	Debug serial clock (270 ohm pull up)
118	SDATA	I/O	Debug serial data (270 ohm pull up)
119	MONI3	O	Internal good title monitor (Connect to TP150)
120	MONI2	O	Internal good title monitor (Connect to TP151)
121	MONI1	O	Internal good title monitor (Connect to TP152)
122	MONI0	O	Internal good title monitor (Connect to TP153)
123	VSS	-	Connect to GND
124	NEJECT	I	Eject detection
125	VDD	-	Power supply 2.7V
126	NTRYCL	I	Non connect (Tray close detection)
127	NDASP	I/O	ATAPI drive active / slave connect I/O
128	NCS3FX	I	Non connect (ATAPI host chip select)
129	NCS1FX	I	Non connect (ATAPI host chip select)
130	VDD	-	Power supply 3V
131	DA2	I/O	ATAPI host address
132	DA0	I/O	Non connect (ATAPI host address)
133	NPDIAG	I/O	ATAPI Slave master diagnosis input
134	VSS	-	Connect to GND
135	DA1	I/O	Non connect (ATAPI host address)
136	NIOCS16	O	Output of selection of width of ATAPI host data bus
137	INTRQ	O	ATAPI Host interruption output
138	VDD	-	Power supply 3V
139	NDMACK	I	Non connect (ATAPI Host DMA characteristic)
140	IORDY	O	ATAPI Host ready output (Connect to TP157)
141	NIORD	I	Non connect (ATAPI host read)
142	VSS	-	Connect to GND
143	NIOWR	I/O	ATAPI Host write
144	DMARQ	O	ATAPI Host DMA request (Connect to TP159)

■ MN101C49GEH (IC500) : AV decorder

1.Terminal layout



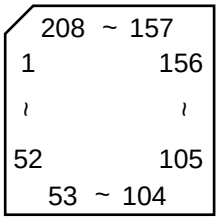
2.Pinfunction

Pin No.	Symbol	I/O	Function
1	VREF	I	Reference voltage
2	NC	-	No connect
3	NC	-	No connect
4	NC	-	No connect
5	NTSEL	I	NTSC/PAL selection
6	POWER SW	-	No connect
7	SHUT1	-	No connect
8	KEY1-5	-	No connect
9	KEY6-10	-	No connect
10	VREF+	I	Reference voltage
11	VDD	I	Power supply
12	OSC2	O	External terminal for connected oscirator
13	OSC1	I	External terminal for connected oscirator
14	VSS	-	Connect to GND
15	XI	I	External terminal for sub oscirator (Supply to voltage)
16	XO	O	No connect
17	MMOD	I	connects with gnd
18	DADATA	I/O	Data bus for DAC
19	DACS1	I/O	Serial bus S1 for DAC
20	DCLK	I/O	Clock for DAC
21	S2UDT	O	Communication between unit microcomputers data output
22	U2SDT	I	Communication between unit microcomputers data output
23	SCLK	I/O	Serial clock bus
24	BUSY	I/O	Busy bus
25	CPURST	O	Unit microcomputer reset
26	REQ	I	Commnication between unit microcomputers REQ
27	REMO	I	Remote control interrruption
28	TEST1	-	Test terminal
29	TEST2	-	Test terminal
30	TEST3	-	Test terminal
31	DVDCS	I	Chip select for DVD
32	NC	-	No connect
33	DVDRST	I	DVD reset
34	NC	-	No connect
35	DACS2	I/O	Serial bus S2 for DAC
36	DACS3	I/O	Serial bus S3 for DAC
37	NC	-	No connect
38	NC	-	No connect
39	FS2	I	Over sampling frequency
40	CHREQ	I	Changer commnication REQUEST
41	CHST	O	Changer commnication STROBE
42	CHDATA	O	Changer commnication DATA I/O
43	NC	-	No connect

Pin No.	Symbol	I/O	Function
44	CHCK	I	Channel clock
45	DVDOUT	O	DVD data output
46	DVDIN	I	DVD data input
47	DVDCLK	I	DVD clock
48	DVDBSY		Busy bus for DVD
49	NC	-	No connect
50	NC	-	No connect
51	NC	-	No connect
52	NC	-	No connect
53	NC	-	No connect
54	VS1	O	Fanction SW control
55	VS3	O	Fanction SW control
56	SL/SRMUTE	O	No connect
57	CMUTE	O	Center signal output mute
58	SWMUTE	O	No connect
59	POB2	O	No connect
60	DEMP2	O	No connect
61	DEMP1	O	No connect
62	DENA	O	No connect
63	KARAOKE	O	No connect
64	POWER ON	O	Power on control output
65	VS2	O	Fanction SW control
66	NC	-	No connect
67	NC	-	No connect
68	NC	-	No connect
69	NC	-	No connect
70	NC	-	No connect
71	NC	-	No connect
72	NC	-	No connect
73	NC	-	No connect
74	NC	-	No connect
75	NC	-	No connect
76	NC	-	No connect
77	AVCI	I	Power supply
78	AVCO	I/O	AV compu link signal I/O port
79	RGB	I	RGB signal in
80	STD	IND	O Standby LED output
81	MPX1	I	MPX1 signal input
82	MPX2	I	MPX2 signal input
83	SRELAY	O	S. Relay control
84	MRELAY	O	M. Relay control
85	BASS1	O	BASS1 switching
86	BASS2	O	BASS2 switching
87	FCD	O	CD power supply control signal
88	PBMUTE	O	PB mute
89	AUXMUTE	O	AUX mute
90	SMUTE	O	System mute output
91	NC	-	No connect
92	NC	-	No connect
93	NC	-	No connect
94	NC	-	No connect
95	DAVSS	-	Connect to GND
96	NC	-	No connect
97	NC	-	No connect
98	NC	-	No connect
99	HPMUTE	O	Head phone mute
100	VREF-	I	Connected GND

■ ZIVA-4.1-PA2 (IC501) : AV decoder

1.Terminal layout



2.Pin function (1/5)

Pin No.	Symbol	I/O	Description
1	RD	I	Read strobe input
2	R/W	I	Read/write strobe input
3	VDD	-	Power supply terminal 3.3V
4	WAIT	O	Transfer not complete / data acknowledge. Active LOW to indicate host initiated transfer is complete.
5	RESET	I	Active LOW : reset signal input
6	VSS	-	Connect to ground
7	VDD	-	Power supply terminal 3.3V
8	INT	O	Host interrupt signal output
9	NC	-	Non connect
10	NC	-	Non connect
11	NC	-	Non connect
12	NC	-	Non connect
13	VDD	-	Power supply terminal 2.5V
14	VSS	-	Connect to ground
15	NC	-	Non connect
16	NC	-	Non connect
17	NC	-	Non connect
18	NC	-	Non connect
19	VSS	-	Connect to ground
20	VDD	-	Power supply 3.3V
21	VDATA0	O	Video data bus output. Byte serial CbYCrY data synchronous with VCLK.
22	VDATA1	O	Video data bus output. Byte serial CbYCrY data synchronous with VCLK.
23	VDATA2	O	Video data bus output. Byte serial CbYCrY data synchronous with VCLK.
24	VDATA3	O	Video data bus output. Byte serial CbYCrY data synchronous with VCLK.
25	VDATA4	O	Video data bus output. Byte serial CbYCrY data synchronous with VCLK.
26	VDATA5	O	Video data bus output. Byte serial CbYCrY data synchronous with VCLK.
27	VDATA6	O	Video data bus output. Byte serial CbYCrY data synchronous with VCLK.
28	VDATA7	O	Video data bus output. Byte serial CbYCrY data synchronous with VCLK.
29	VSYNC	I/O	Vertical sync. Bi-directional, the decoder output the top border of a new field on the first HSYNC after the falling edge of VSYNC.
30	HSYNC	I/O	Horizontal sync. The decoder begins outputting pixel data for a new horizontal line after the falling (active) edge of HSYNC.
31	VSS	-	Connect to ground
32	VDD	-	Power supply terminal 3.3V
33	NC	-	Non connect
34	NC	-	Non connect
35	NC	-	Non connect
36	VDD	-	Power supply terminal 2.5V

2.Pin function (2/5)

Pin No.	Symbol	I/O	Description
37	VSS	-	Connect to ground
38	NC	-	Non connect
39	NC	-	Non connect
40	NC	-	Non connect
41	NC	-	Non connect
42	NC	-	Non connect
43	PIO0	I/O	Programmable I/O terminal
44	VSS	-	Connect to ground
45	VDD	-	Power supply terminal 3.3V
46	PIO1	I/O	Programmable I/O terminal
47	PIO2	I/O	Programmable I/O terminal
48	PIO3	I/O	Programmable I/O terminal
49	PIO4	I/O	Programmable I/O terminal
50	PIO5	I/O	Programmable I/O terminal
51	PIO6	I/O	Programmable I/O terminal
52	PIO7	I/O	Programmable I/O terminal
53	MDATA0	I/O	SDRAM data
54	MDATA1	I/O	SDRAM data
55	VDD	-	Power supply terminal 3.3V
56	VSS	-	Connect to ground
57	MDATA2	I/O	SDRAM data
58	MDATA3	I/O	SDRAM data
59	MDATA4	I/O	SDRAM data
60	MDATA5	I/O	SDRAM data
61	MDATA6	I/O	SDRAM data
62	MDATA7	I/O	SDRAM data
63	MDATA15	I/O	SDRAM data
64	VDD	-	Power supply terminal 3.3V
65	VSS	-	Connect to ground
66	MDATA14	I/O	SDRAM data
67	VDD	-	Power supply terminal 2.5
68	VSS	-	Connect to ground
69	MDATA13	I/O	SDRAM data
70	MDATA12	I/O	SDRAM data
71	MDATA11	I/O	SDRAM data
72	MDATA10	I/O	SDRAM data
73	MDATA9	I/O	SDRAM data
74	VDD	-	Power supply terminal 3.3V
75	VSS	-	Connect to ground
76	MDATA8	I/O	SDRAM data
77	LDQM	O	SDRAM Lower or upper mask
78	SD-CLK	O	SDRAM Clock
79	CLKSEL	I	Selects SYSCLK or VCLK as clock source. Normal operation is to tie HIGH.
80	MADDR9	O	SDRAM address
81	MADDR8	O	SDRAM address
82	VDD	-	Power supply terminal 3.3V
83	VSS	-	Connect to ground
84	MADDR7	O	SDRAM address

2.Pin function (3/5)

Pin No.	Symbol	I/O	Description
85	MADDR6	O	SDRAM address
86	MADDR5	O	SDRAM address
87	VDD	-	Power supply terminal 2.5V
88	VSS	-	Connect to ground
89	MADDR4	O	SDRAM address
90	MWE	O	SDRAM write enable
91	SD-CAS	O	Active LOW SDRAM column address
92	VDD	-	Power supply terminal 3.3V
93	VSS	-	Connect to ground
94	SD-RAS	O	Active LOW SDRAM row address
95	SD-CS0	O	Active LOW SDRAM chip select 0
96	SD-CS1/MADDR11	O	Active LOW SDRAM chip select 1 or use as MADDR11 for larger SDRAM
97	SD-BS	O	SDRAM bank select
98	MADDR10	O	SDRAM address
99	MADDR0	O	SDRAM address
100	VDD	-	Power supply terminal 3.3V
101	VSS	-	Connect to ground
102	MADDR1	O	SDRAM address
103	MADDR2	O	SDRAM address
104	MADDR3	O	SDRAM address
105	RESERVED	I	Tie to VSS or VDD_3.3 as specified in table1
106	NC	-	Non connect
107	NC	-	Non connect
108	RESERVED	I	Tie to VSS or VDD_3.3 as specified in table1
109	NC	-	Non connect
110	RESERVED	I	Tie to VSS or VDD_3.3 as specified in table1
111	RESERVED	I	Tie to VSS or VDD_3.3 as specified in table1
112	RESERVED	I	Tie to VSS or VDD_3.3 as specified in table1
113	DAI-LRCK	I	PCM left/right clock
114	DAI-BCK	I	PCM input bit clock
115	VDD	-	Power supply 3.3V
116	VSS	-	Connect to ground
117	DAI-DATA	I	PCM data input
118	DA-DATA3	O	PCM data output. Eight channels. Serial audio samples relative to DA_BCK and DA_LRCK
119	DA-DATA2	O	PCM data output. Eight channels. Serial audio samples relative to DA_BCK and DA_LRCK
120	DA-DATA1	O	PCM data output. Eight channels. Serial audio samples relative to DA_BCK and DA_LRCK
121	DA-DATA0	O	PCM data output. Eight channels. Serial audio samples relative to DA_BCK and DA_LRCK
122	DA-LRCK	O	PCM left clock. Identifies the channel for each sample
123	VDD	-	Power supply terminal 3.3V
124	VSS	-	Connect to ground
125	DA-XCK	I/O	Audio external frequency clock input or output
126	DA-BCK	O	PCM bit clock output
127	DA-IEC	O	PCM data out in IEC-958 format or compressed data out in IEC-1937 format
128	VDD	-	Power supply terminal 2.5V

2.Pin function (4/5)

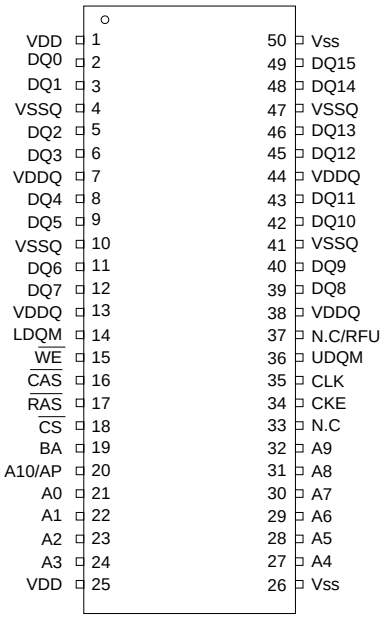
Pin No.	Symbol	I/O	Description
129	VSS	-	Connect to ground
130	NC	-	Non connect
131	VSS_DAC	-	Connect to ground for analog video DAC
132	VSS_VIDEO	-	Connect to ground for analog video
133	CVBS	O	DAC video output format : CVBS. Macrovision encoded
134	VDD_DAC	-	Power supply terminal for analog video DAC
135	VDD_VIDEO	-	Power supply terminal for analog video
136	NC	-	Non connect
137	VSS_DAC	-	Connect to ground for analog video DAC
138	VSS_VIDEO	-	Connect to ground for analog video
139	CVBS/G/Y	O	DAC video output format. Macrovision encoded
140	VDD_DAC	-	Power supply terminal for analog video DAC
141	VDD_VIDEO	-	Power supply terminal for analog video
142	NC	-	Non connect
143	VSS_DAC	-	Connect to ground for analog video DAC
144	VSS_VIDEO	-	Connect to ground for analog video
145	Y/B/U	O	DAC video output format. Macrovision encoded
146	VDD_DAC	-	Power supply terminal for analog video DAC
147	VDD_VIDEO	-	Power supply terminal for analog video
148	NC	-	Non connect
149	VSS_DAC	-	Connect to ground for analog video DAC
150	VSS_VIDEO	-	Connect to ground for analog video
151	C/R/V	O	DAC video output format. Macrovision encoded
152	VDD_DAC	-	Power supply terminal for analog video DAC
153	VDD_VIDEO	-	Power supply terminal for analog video
154	VSS_RREF	-	Connect to ground for analog video
155	RREF	O	Reference resistor. Connecting to pin 154
156	VDD_RREF	-	Power supply terminal for analog video 3.3V
157	A_VSS	-	Power supply terminal for analog PLL 3.3V
158	SYSCLK	I	Optical system clock. Tie to A_VDD through a 1K ohm resistor
159	VCLK	I	System clock input
160	A_VDD	-	Power supply terminal for analog PLL 3.3V
161	DVD-DATA0/CD-DATA	I	Serial CD data. This pin is shared with DVD compressed data DVD-DATA0
162	DVD-DATA1/CD-LRC	I	Programmable polarity 16-bit word synchronization to the decoder. This pin is shared with DVD compressed data DVD-DATA1
163	DVD-DATA2/CD-BCK	I	CD bit clock. Decoder accept multiple BCK rates. This pin is shared with DVD compressed DVD-DATA2
164	DVD-DATA3/CD-C2PO	I	Asserted HIGH indicates a corrupted byte. This pin is shared with DVD compressed data DVD-DATA3
165	DVD-DATA4/CDGSDATA	I	DVD parallel compressed data from DVD DSP. or CD-G data indicating serial subcode data input
166	VSS	-	Connect to ground
167	VDD	-	Power supply terminal 3.3V
168	DVD-DATA5/CDG-VFSY	I	DVD parallel compressed data from DVD DSP. or CD-G frame sync indicating frame-start or composite synchronization input.
169	DVD-DATA6/CDG-SOS1	I	DVD parallel compressed data from DVD DSP. or CD-G block sync indicating block-start synchronization input

2.Pin function (5/5)

Pin No.	Symbol	I/O	Description
170	DVD-DATA7/CDG-SCLK	I	DVD parallel compressed data from DVD DSP. or CD-G clock indicating sub code data clock input or output
171	VDACK	I	In synchronous mode, bitstream data acknowledge. Asserted when DVD data is valid.Polarity is programmable
172	VREQUEST	O	Bitstream request
173	VSTROBE	I	Bitstream strobe
174	ERROR	I	Error in input data
175	VDD	-	Power supply terminal 3.3V
176	RESERVED	I	Tie to VSS or VDD_3.3 as specified in table 1
177	VDD	-	Power supply terminal 3.3V
178	VSS	-	Connect to ground
179	NC	-	Non connect
180	RESERVED	I	Tie to VSS or VDD_3.3 as specified in table 1
181	NC	-	Non connect
182	HADDR0	I	Host addressbus. 3-bit address bus selects one of eight host interface registers
183	HADDR1	I	Host addressbus. 3-bit address bus selects one of eight host interface registers
184	HADDR2	I	Host addressbus. 3-bit address bus selects one of eight host interface registers
185	RESERVED	I	Tie to VSS or VDD_3.3 as specified in table 1
186	RESERVED	I	Tie to VSS or VDD_3.3 as specified in table 1
187	RESERVED	I	Tie to VSS or VDD_3.3 as specified in table 1
188	VSS	-	Connect to ground
189	VDD	-	Power supply terminal 2.5V
190	RESERVED	I	Tie to VSS or VDD_3.3 as specified in table 1
191	VSS	-	Connect to ground
192	VDD	-	Power supply terminal 3.3V
193	RESERVED	I	Tie to VSS or VDD_3.3 as specified in table 1
194	RESERVED	I	Tie to VSS or VDD_3.3 as specified in table 1
195	RESERVED	I	Tie to VSS or VDD_3.3 as specified in table 1
196	RESERVED	I	Tie to VSS or VDD_3.3 as specified in table 1
197	HDATA7	I/O	The 8-bit bi-derectional host data through which the host writes data to the decoder code.
198	VSS	-	Connect to ground
199	HDATA6	I/O	The 8-bit bi-derectional host data through which the host writes data to the decoder code.
200	HDATA5	I/O	The 8-bit bi-derectional host data through which the host writes data to the decoder code.
201	HDATA4	I/O	The 8-bit bi-derectional host data through which the host writes data to the decoder code.
202	HDATA3	I/O	The 8-bit bi-derectional host data through which the host writes data to the decoder code.
203	HDATA2	I/O	The 8-bit bi-derectional host data through which the host writes data to the decoder code.
204	VDD	-	Power supply terminal 3.3V
205	VSS	-	Connect to ground
206	HDATA1	I/O	The 8-bit bi-derectional host data through which the host writes data to the decoder code.
207	HDATA0	I/O	The 8-bit bi-derectional host data through which the host writes data to the decoder code.
208	CS	I	Host chip select input

■ KM416S1120DT-G8 or W981616AH-7 (IC504,IC505) : 16M SDRAM

1.Terminal layout

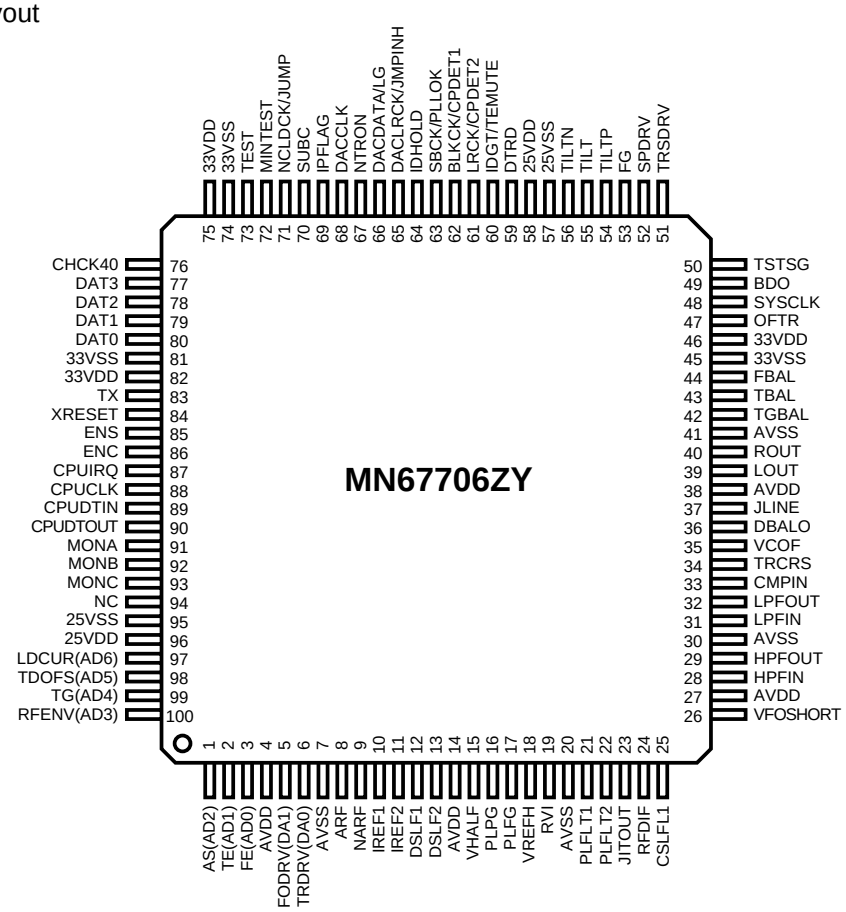


2.Pin function

Pin No.	Symbol	I/O	Function	Pin No.	Symbol	I/O	Function
1	VCC	-	Power supply	26	VSS	-	Connect to GND
2	DQ0	I/O	Data input/output	27	A4	I	Address input
3	DQ1	I/O	Data input/output	28	A5	I	Address input
4	VSSQ	-	Connect to GND	29	A6	I	Address input
5	DQ2	I/O	Data input/output	30	A7	I	Address input
6	DQ3	I/O	Data input/output	31	A8	I	Address input
7	VSSQ	-	Power supply	32	A9	I	Address input
8	DQ4	I/O	Data input/output	33	NC	-	No connect
9	DQ5	I/O	Data input/output	34	CKE	I	Clock enable
10	VSSQ	-	Connect to GND	35	CLK	I	System clock input
11	DQ6	I/O	Data input/output	36	UDQM	O	Data input/output mask
12	DQ7	I/O	Data input/output	37	NC	-	No connect
13	VCCQ	-	Power supply	38	VCCQ	-	Power supply
14	LDQM	O	Data input/output mask	39	DQ8	I/O	Data input/output
15	-WE	I	Write enable	40	DQ9	I/O	Data input/output
16	-CAS	I	Colum address strobe	41	VSSQ	-	Connect to GND
17	-RAS	I	Row addres strobe	42	DQ10	I/O	Data input/output
18	CS	I	Chip select	43	DQ11	I/O	Data input/output
19	A11		Bank select adress	44	VCCQ	-	Power supply
20	A10	I	Address input	45	DQ12	I/O	Data input/output
21	A0	I	Address input	46	DQ13	I/O	Data input/output
22	A1	I	Address input	47	VSSQ	-	Connect to GND
23	A2	I	Address input	48	DQ14	I/O	Data input/output
24	A3	I	Address input	49	DQ15	I/O	Data input/output
25	VCC	-	Power supply	50	VSS	-	Connect to GND

■ MN67706ZY (IC201) : Auto digital servo controller

1.Terminal layout



2.Pin functions (1/3)

Pin No.	Symbol	I/O	Function
1	AS(AD2)	I	AS : Full adder signal(FEP)
2	TE(AD1)	I	Phase difference/3 beam tracking error(FEP)
3	FE(AD0)	I	Focus error(FEP)
4	AVDD	-	Apply 3.3V(For analog circuit)
5	FODRV(DA1)	O	Focus drive(DRVIC)
6	TRDRV(DA0)	O	Tracking drive(DRVIC)
7	AVSS	-	Ground(For analog circuit)
8	ARF	I	Equivalence RF+(FEP)
9	NARF	I	Equivalence RF-(FEP)
10	IREF1	I	Reference current1(For DBAL)
11	IREF2	I	Reference current2(For DBAL)
12	DSLF1	I/O	Connect to capacitor1 for DSL
13	DSLF2	I/O	Connect to capacitor2 for DSL
14	AVDD	-	Apply 3.3V(For analog circuit)
15	VHALF	I	Reference voltage 1.65+-0.1V(FEP)
16	PLPG	-	Not use(PLL phase gain setting resistor terminal)
17	PLFG	-	Not use(PLL frequency gain setting resistor terminal)
18	VREFH	I	Reference voltage 2.2V+-0.1V(FEP)
19	RVI	I/O	Connect to resistor for VREFH reference current source
20	AVSS	-	Ground(For analog circuit)
21	PLFLT1	O	Connect to capacitor1 for PLL
22	PLFLT2	O	Connect to capacitor2 for PLL
23	JITOUT	I/O	Output for jitter signal monitor
24	RFDIF	I	Not use
25	CSLFL1	I/O	Pull-up to VHALF

2.Pin function (2/3)

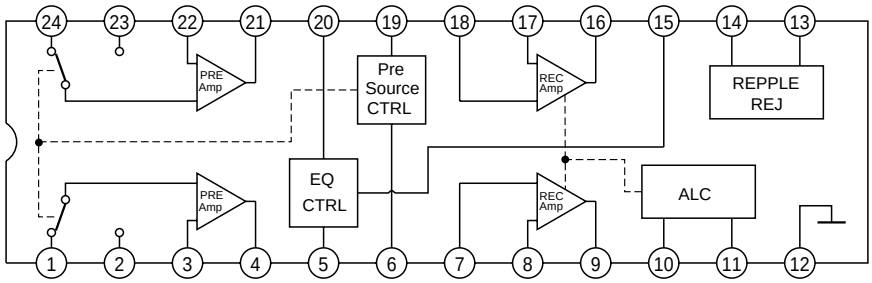
Pin No.	Symbol	I/O	Function
26	VFOSHORT	O	VFO short output
27	AVDD	-	Apply 3.3V(For analog circuit)
28	HPFIN	I	Pull-up to VHALF
29	HPFOUT	O	Connect to TP208
30	AVSS	-	Ground(For analog circuit)
31	LPFIN	I	Pull-up to VHALF
32	LPFOUT	O	Not use
33	CMPIN	I	Connect to TP210
34	TRCRS	I	Input signal for track cross formation
35	VCOF	I/O	JFVCO control voltage
36	DBALO	O	DSL balance adjust output
37	JLINE	O	J-line setting output(FEP)
38	AVDD	-	Apply 3.3V(For analog circuit)
39	LOUT	O	Connect to TP203 (Analog audio left output)
40	ROUT	O	Connect to TP204 (Analog audio right output)
41	AVSS	-	Ground(For analog circuit)
42	TGBAL	O	Tangential balance adjust(FEP)
43	TBAL	O	Tracking balance adjust(FEP)
44	FBAL	O	Focus balance adjust(FEP)
45	33VSS	-	Ground(For I/O)
46	33VDD	-	Apply 3.3V(For I/O)
47	OFTR	I	Off track signal
48	SYSCLK	I	16.9344MHz system clock input(ODC)
49	BDO	I	Drop out(FEP)
50	TSTSG	O	Calibration signal(FEP)
51	TRSDRV	O	Traverse drive(DRVIC)
52	SPDRV	O	Spindle drive output(DRVIC)
53	FG	I	FG signal input (Spindle motor driver)
54	TILTP	O	Connect to TP205
55	TILT	O	Connect to TP206
56	TILTN	O	Connect to TP207
57	25VSS	-	Ground(For internal core)
58	25VDD	-	Apply 2.5V(For internal core)
59	DTRD	I	Data read control signal(ODC)
60	IDGT/TEMUTE	I	Pull-down to Ground
61	LRCK/CPDET2	O	LR channel data strobe(ODC)/
62	BLKCK/CPDET1	O	CD sub code synchronous signal(ODC)/
63	SBCK/PLLOK	I	CD sub code data shift clock(ODC)/PLL pull-in OK signal input
64	IDHOLD	I	Pull-down to Ground
65	DACLRCK/JMPINH	I	1bit DAC-LR channel data strobe(ODC)/
66	DACDATA/LG	I	CD 1bit DAC channel data(ODC)
67	NTRON	O	L : Tracking ON(ODC)
68	DACCLK	O	1bit DAC channel data shift clock(ODC)
69	IPFLAG	O	CIRC error flag(ODC)
70	SUBC	O	CD sub code(ODC)
71	NCLDCK/JUMP	O	CD sub code data frame clock(ODC)/DVD JUMP signal(ODC)
72	MINTEST	I	Pull-down to Ground(For MINTEST)
73	TEST	I	Pull-down to Ground(For TEST)
74	33VSS	-	Ground(For I/O)
75	33VDD	-	Apply 3.3V(For I/O)
76	CHCK40	O	Clock for SRDATA(ODC)
77	DAT3	O	SRDATA3(ODC)
78	DAT2	O	SRDATA2(ODC)
79	DAT1	O	SRDATA1(ODC)
80	DAT0	O	SRDATA0(ODC)

2.Pin function (3/3)

Pin No.	Symbol	I/O	Function
81	33VSS	-	Ground(For I/O)
82	33VDD	-	Apply 3.3V(For I/O)
83	TX	O	Digital audio interface
84	XRESET	I	Reset input (System control)
85	ENS	I	Servo DSC serial I/F chip select (System control)
86	ENC	I	CIRC serial I/F chip select (System control)
87	CPUIRQ	O	Interrupt request (System control)
88	CPUCLK	I	Syscon serial I/F clock (System control)
89	CPUDTIN	I	Syscon serial I/F data input (System control)
90	CPUDTOUT	O	Syscon serial I/F data output (System control)
91	MONA	O	Connect to TP226 (Monitor terminal A)
92	MONB	O	Connect to TP225 (Monitor terminal A)
93	MONC	O	Connect to TP224 (Monitor terminal A)
94	NC	O	Connect to TP211
95	25VSS	-	Ground(For internal core)
96	25VDD	-	Apply 2.5V(For internal core)
97	LDCUR(AD6)	I	
98	TDOFS(AD5)	I	
99	TG(AD4)	I	Tangential phase difference(FEP)
100	RFENV(AD3)	I	RF envelope input(FEP)

■ AN7345K (IC302) : REC/PRE amp

1.Terminal layout & block diagram

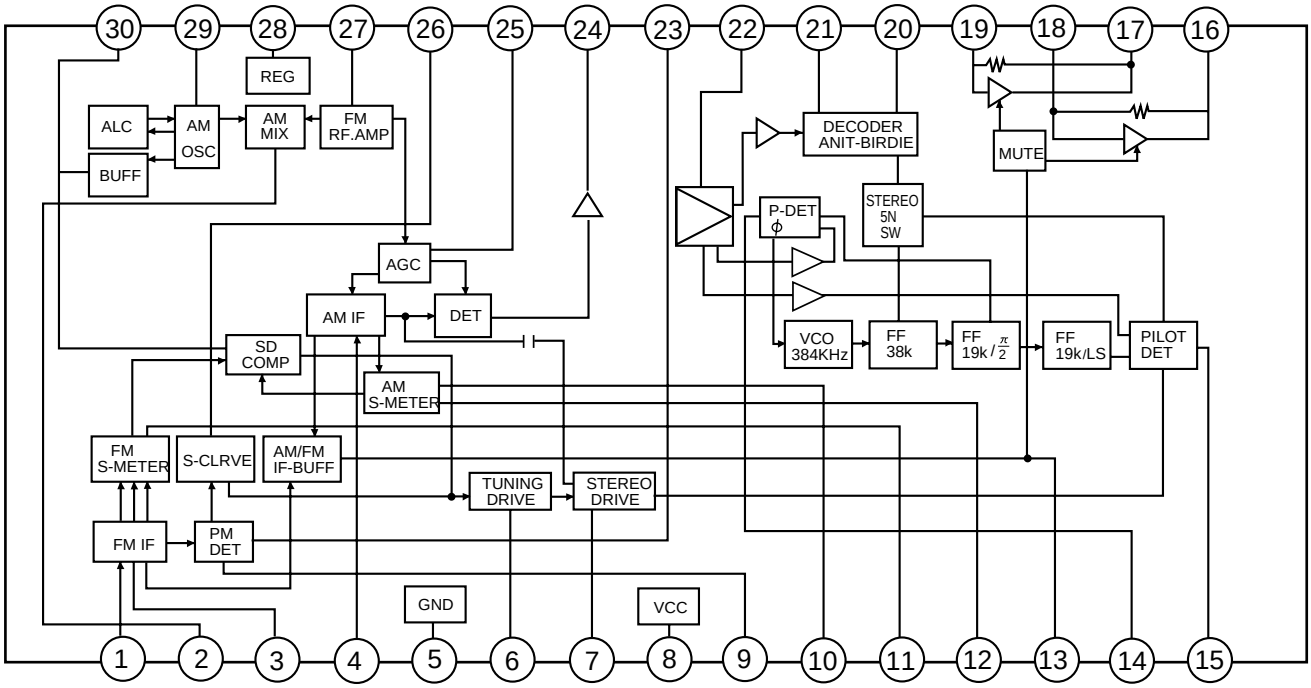


2.Pin function

Pin No.	I/O	Function
1	I	CH1 Playback amplifier input(1)
2	I	CH1 Playback amplifier input(2)
3	I	CH1 Playback amplifier negative feedback
4	O	CH1 Playback amplifier output
5	I	CH1 Equalizer input
6	O	Pre amplifier input control time constant
7	I	CH1 Recoding amplifier input
8	I	CH1 Recoding amplifier negative output
9	O	CH1 Recoding amplifier output
10	O	ALC low cut
11	O	ALC L.P.F
12	-	Connect to GND
13	-	Power supply
14	O	Repple filter
15	I	Equalizer control
16	O	CH2 Recoding amplifier output
17	I	CH2 Recoding amplifier negative output
18	I	CH2 Recoding amplifier input
19	O	Pre amplifier input control
20	I	CH2 Equalizer input
21	O	CH2 Playback amplifier output
22	I	CH2 Playback amplifier negative feedback
23	I	CH2 Playback amplifier input(2)
24	I	CH2 Playback amplifier input(1)

■ LA1838 (IC102) : FM AM IF AMP & Detector, FM MPX Decoder

1. Block diagram

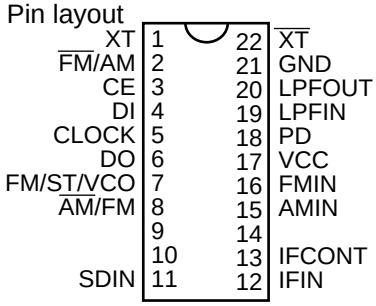


2. Pin function

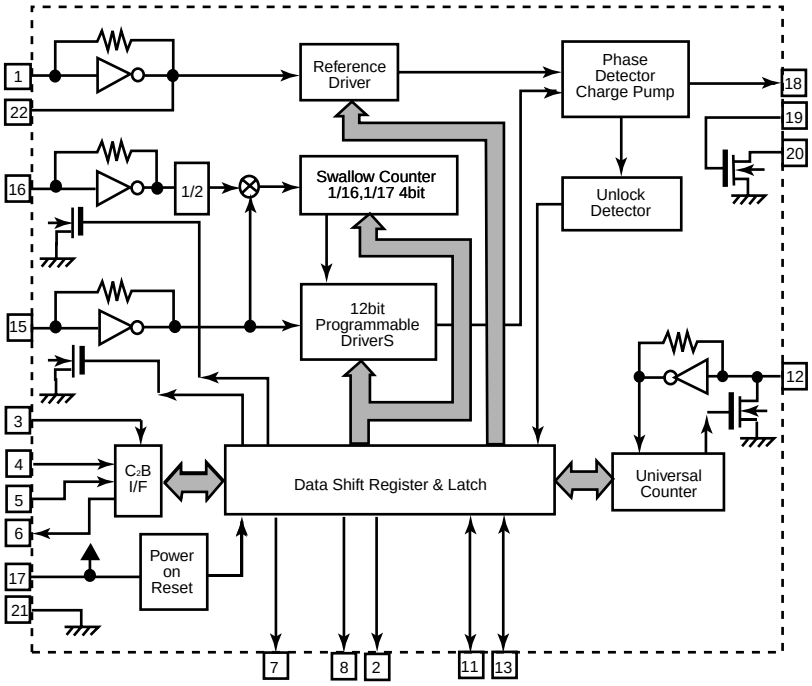
Pin No.	Symbol	I/O	Function	Pin No.	Symbol	I/O	Function
1	FM IN	I	This is an input terminal of FM IF signal.	16	L OUT	O	Left channel signal output.
2	AM MIX	O	This is an out put terminal for AM mixer.	17	R OUT	O	Right channel signal output.
3	FM IF	I	Bypass of FM IF	18	L IN	I	Input terminal of the Left channel post AMP.
4	AM IF	I	Input of AM IF Signal.	19	R IN	I	Input terminal of the Right channel post AMP.
5	GND	—	This is the device ground terminal.	20	RO	O	Mpx Right channel signal output.
6	$\overline{\text{TUNED}}$	O	When the set is tunning,this terminal becomes "L".	21	LO	O	Mpx Left channel signal output.
7	$\overline{\text{STEREO}}$	O	Stereo indicator output. Stereo "L", Mono: "H"	22	MPX IN	I	Mpx input terminal
8	VCC	—	This is the power supply terminal.	23	FM OUT	O	FM detection output.
9	FM DET	—	FM detect transformer.	24	AM DET	O	AM detection output.
10	AM SD	—	This is a terminal of AM ceramic filter.	25	AM AGC	I	This is an AGC voltage input terminal for AM
11	FM VSM	O	Adjust FM SD sensitivity.	26	AFC	—	This is an output terminal of voltage for FM-AFC.
12	AM VSM	O	Adjust AM SD sensitivity.	27	AM RF	I	AM RF signal input.
13	MUTE	I/O	When the signal of IF REQ of IC121(LC72131) appear, the signal of FM/AM IF output. //Muting control input.	28	REG	O	Register value between pin 26 and pin28 besides the frequency width of the input signal.
14	FM/$\overline{\text{AM}}$	I	Change over the FM/AM input. "H" :FM, "L" : AM	29	AM OSC	—	This is a terminal of AM Local oscillation circuit.
15	$\overline{\text{MONO}}$/ST	O	Stereo : "H", Mono: "L"	30	OSC BUFFER	O	AM Local oscillation Signal output.

■ LC72136N (IC2) : PLL Frequency synthesizer

1. Pin layout



2. Block diagram

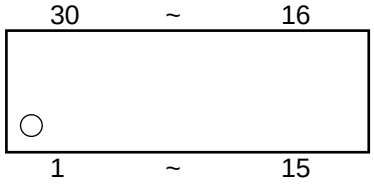


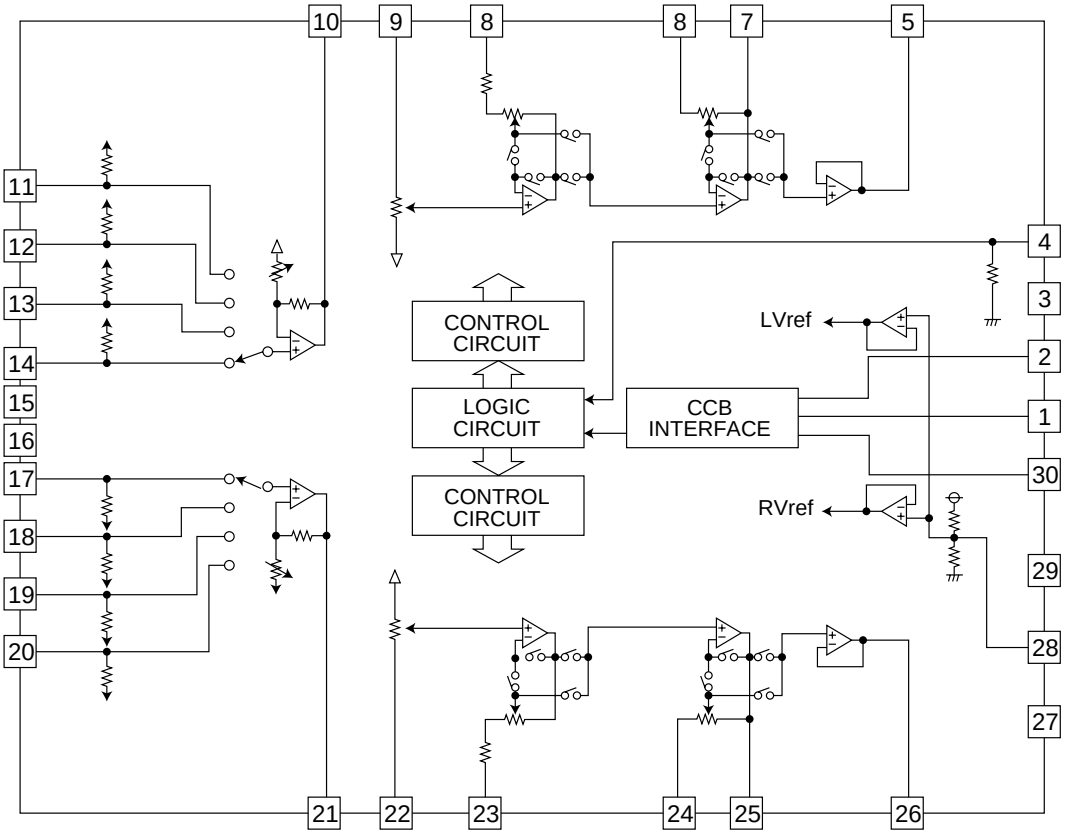
3. Pin function

Pin No.	Symbol	I/O	Function	Pin No.	Symbol	I/O	Function
1	XT	I	X'tal oscillator connect (75kHz)	12	IFIN	I	IF counter signal input
2	$\overline{FM}$/AM	O	LOW:FM mode	13	IFCONT	O	IF signal output
3	CE	I	When data output/input for 4pin(input) and 6pin(output): H	14		-	Not use
4	DI	I	Input for receive the serial data from controller	15	AMIN	I	AM Local OSC signal output
5	CLOCK	I	Sync signal input use	16	FMIN	I	FM Local OSC signal input
6	DO	O	Data output for Controller Output port	17	VCC	-	Power suplly(VDD=4.5-5.5V) When power ON:Reset circuit move
7	FM/ST/VCO	O	"Low": MW mode	18	PD	O	PLL charge pump output(H: Local OSC frequency Height than Reference frequency. L: Low Agreement: Height impedance)
8	$\overline{AM}$/FM	O	Open state after the power on reset	19	LPFIN	I	Input for active lowpassfilter of PLL
9	LW	I/O	Input/output port	20	LPFOUT	O	Output for active lowpassfilter of PLL
10	MW	I/O	Input/output port	21	GND	-	Connected to GND
11	SDIN	I/O	Data input/output	22	$\overline{XT}$	I	X'tal oscillator(75KHz)

■LC75342M-X (IC301) : E. volume

1. Terminal layout



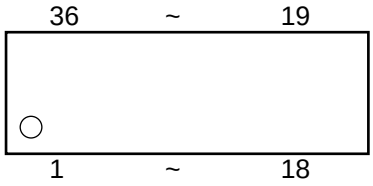


3. Pin function

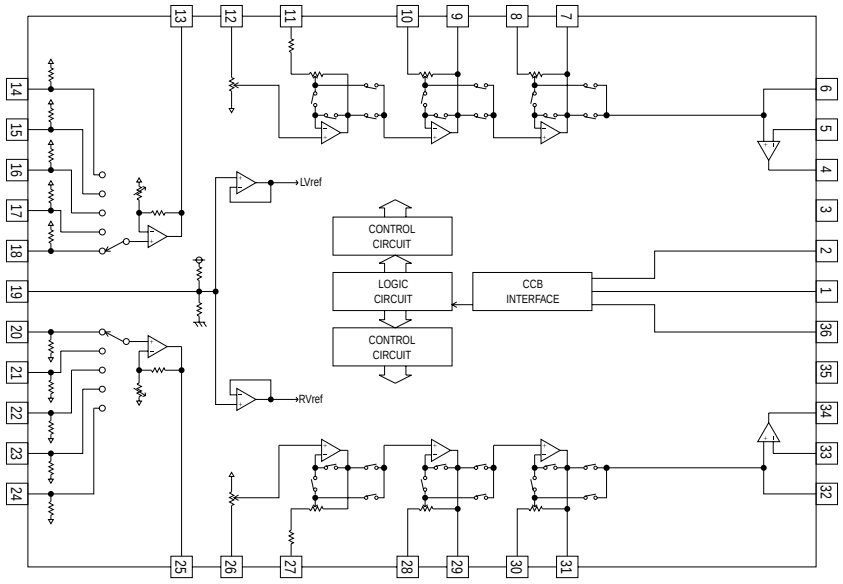
Pin No.	Symbol	Function	Pin No.	Symbol	Function
1	DI	Serial data and clock input for IC control	17	R1	Input signal connections
2	CE	Chip enable	18	R2	Input signal connections
3	VSS	Connect to GND	19	R3	Input signal connections, not used
4	TEST	Electric volume connection for test	20	R4	Not used
5	LOUT	Volume control and equalizer input	21	RSEL0	Input selector output
6	LBASS2	Connection for resistor and capacitor that	22	RIN	Volume control and equalizer input
7	LBASS1	from the bass band filter	23	RTRE	Connection for capacitor that from the treble band filter
8	LTRE	Connection for capacitor that from the treble band filter	24	RBASS1	Connection for resistor and capacitor that from the bass band filter
9	LIN	Volume control and equalizer input	25	RBASS2	
10	LSEL0	Input selector output	26	ROUT	Volume control and equalizer input
11	L4	Not used	27	NC	Not used
12	L3	Input signal connections, not used	28	VREF	Connection to the 0.5X VDD voltage generator circuit used as the analog signal ground
13	L2	Input signal connections			
14	L1	Input signal connections	29	VDD	Power supply
15	NC	Connect to GND	30	CL	Serial data and clock input for IC control
16	NC	Connect to GND			

■ LC75345M-X (IC521) : Input selector

1.Terminal layout



2.Block diagram

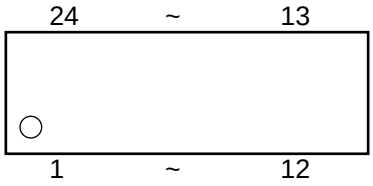


3. Pin function

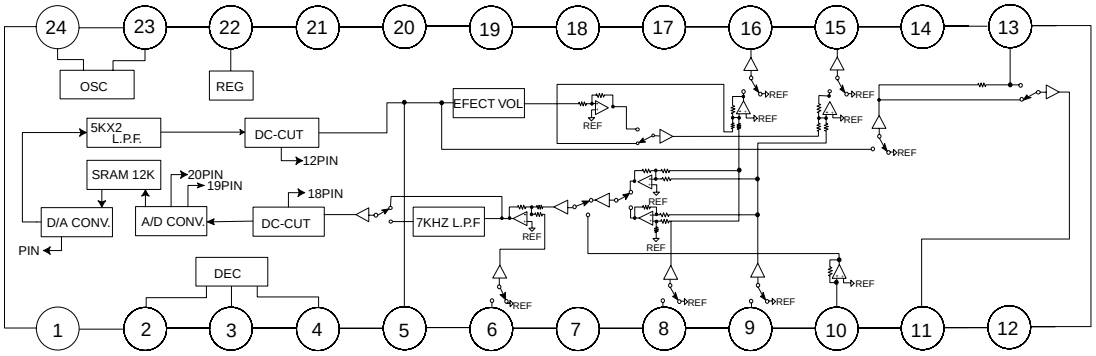
Pin No.	Symbol	Function	Pin No.	Symbol	Function
1	DI	Serial data input	19	VREF	0.5 X VDD voltage genration block for analog ground
2	CE	Chip enable			
3	VSS	Connect to GND	20	DVDR	DVD Rch signal input pin
4	LOPOUT	Output pin of genral purpose operation amplifier	21	PBR	Playback Rch signal input pin
			22	TUR	Tuner Rch signal input pin
5	LINM	Non-inverterd pin of general purpose operation amplifier	23	AUXR	Aux Rch signal input pin
			24	NC	No connect
6	NC	No connect	25	RSEL0	Input selector output pin
7	LOUT	Att + equalizer output	26	RIN	Volume input
8	LSB	Capacitor and resistor connection pins comprising filters for bass and super-bass band	27	RTRE	Capacitor connection pin comprising terble band filter
9	LBASS2				
10	LBASS1		28	RBASS1	Capacitor and resistor connection
11	LTRE	Capacitor connection pin comprising treble band filter	29	RBASS2	pins comprising
			30	RSB	filters for bass and superbass band
12	LIN	Volume input	31	ROUT	Att + equalizer output
13	LSEL0	Input selector output pin	32	NC	No connect
14	NC	No connect	33	RINM	Non-inverterd pin of general purpose operation amplifier
15	AUXL	Aux Lch signal input pin			
16	TUL	Tuner Lch signal input pin	34	ROPOUT	Output pin of genral purpose operation amplifier
17	PBL	Playback Lch signal input pin			
18	DVDL	DVD Lch signal input pin	35	VDD	Power supply
19		0.5 X VDD voltag genration block for analog ground	36	CL	Clock input

■ LV1100M (IC550) : Karaoke mic echo surround amp.

1.Terminal layout



2.Block diagram

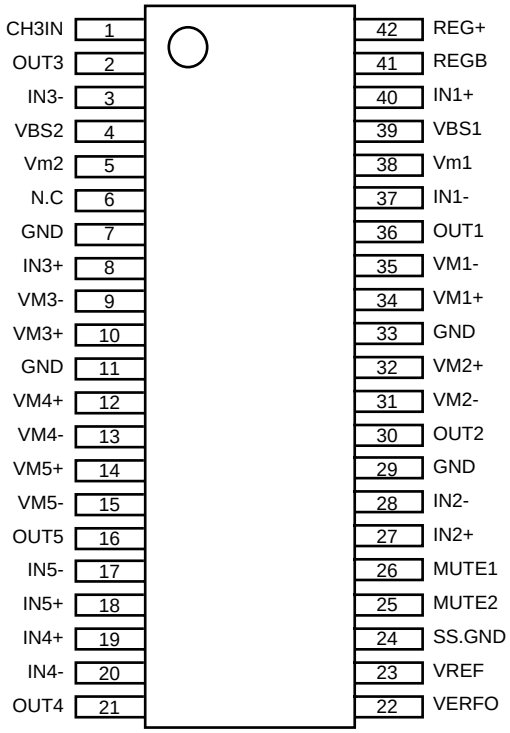


3. Pin function

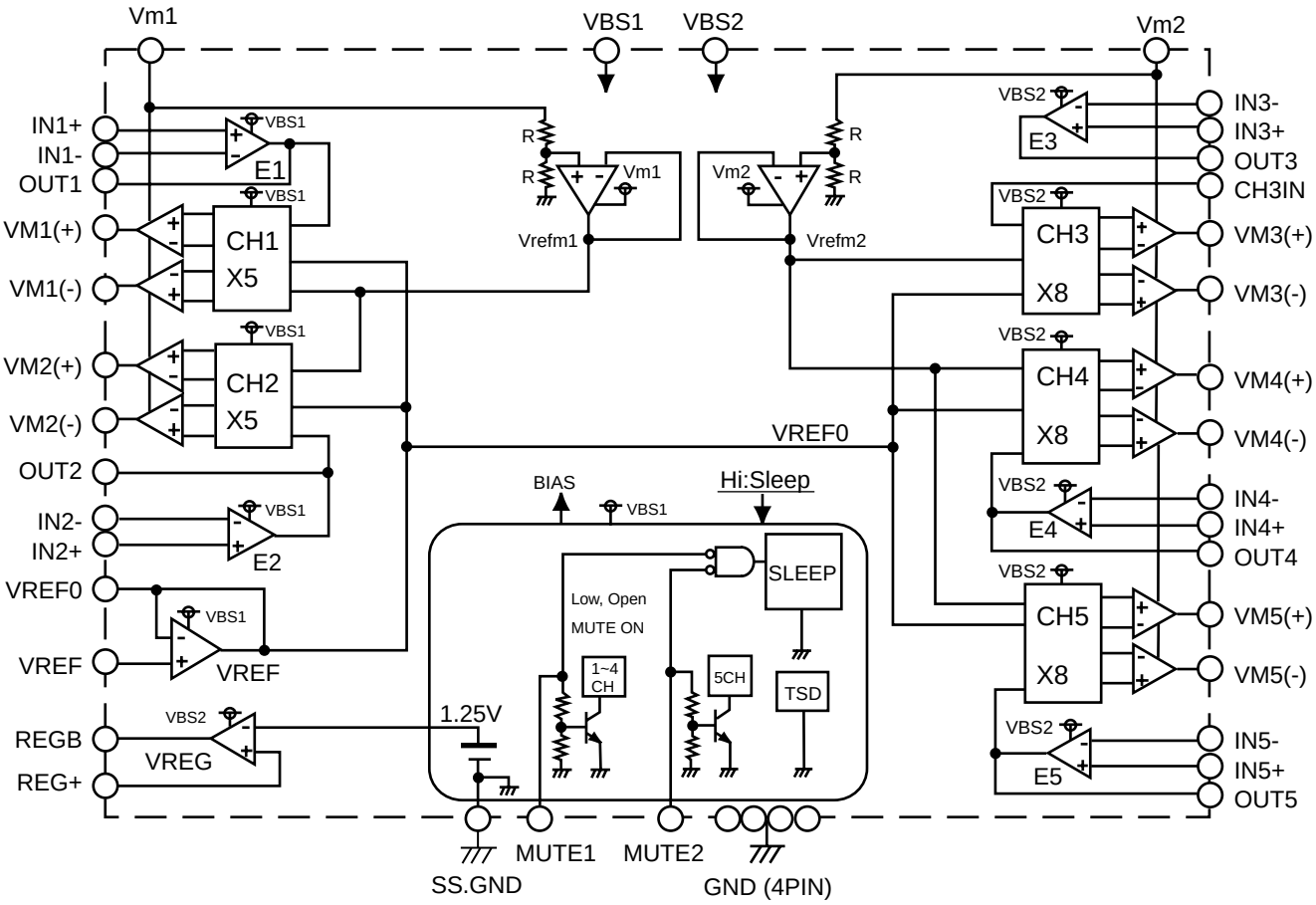
Pin No.	Symbol	I/O	Function
1	VSS	-	Connect to GND
2	CLOCK	I	Clock for communicated data
3	DATA	I	Amp. control data
4	ENABLE	I	Control signal enable
5	REV-OUT	O	Reverse signal output
6	REV-IN	I	Reverse signal input
7	VCC	-	Power supply
8	IN-L	I	Analog signal input L
9	IN-R	I	Analog signal input R
10	IN-A	I	N.C.
11	OUT-A	O	N.C.
12	DC-OUT	O	DC-output
13	LPF	I	External terminal for low pass filter
14	VREF	I	Reference voltage
15	OUT-R	O	Analog signal output R
16	OUT-L	O	Analog signal output L
17	AGND	-	Connect to GND
18	DC-OUT	O	DC-output
19	A/D	I	External terminal for A/D
20	A/D	I	External terminal for A/D
21	D/A	I	External terminal for D/A
22	VDD	-	Power supply
23	X2	O	External terminal for oscillator
24	X1	I	External terminal for oscillator

M56788FP-W (IC271) : Traverse mechanism driver

1.Terminal layout

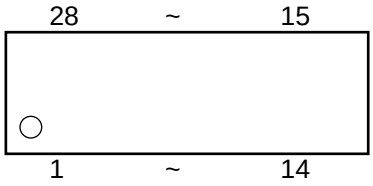


2.Block diagram



■ MN35505 (IC501,IC502,IC503) : DAC

1.Terminal layout

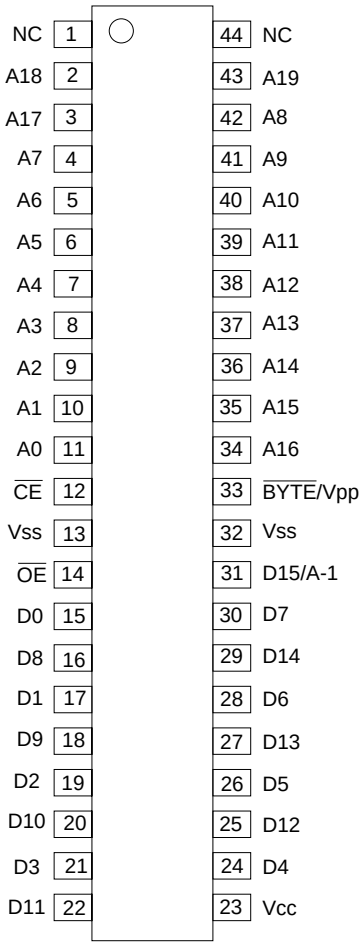


2. Pin function

Pin No.	Symbol	I/O	Function
1	M5	I	Control signal for DAC
2	DIN	I	Digital data input
3	LRCK	I	L and R clock for DAC
4	BCK	I	Bit clock for DAC
5	M3	I	Control signal for DAC
6	DVDD2	-	Power supply
7	CKO	-	No connect
8	DVSS2	-	Connect to GND
9	M2	I	Control signal for DAC
10	M1	I	Control signal for DAC
11	OUT1C	O	Analog output 1
12	AVDD1	-	Power supply
13	OUT1D	O	Analog output 1
14	AVSS1	-	Connect to GND
15	AVSS2	-	Connect to GND
16	OUT2D	O	Analog output 2
17	AVDD2	-	Power supply
18	OUT2C	O	Analog output 2
19	M9	I	Control signal for DAC
20	DVSS2	-	Connect to GND
21	XOUT	-	No connect
22	XIN	-	No connect
23	VCOF	I	VCO frequency
24	DVDD1	-	Power supply D+5V
25	M7	-	Connect to GND
26	M8	-	Connect to GND
27	M4	I	Control signal for DAC
28	M6	I	Clock for control signal

■ MR27V1602ESIMAX (IC402) : 16M ROM

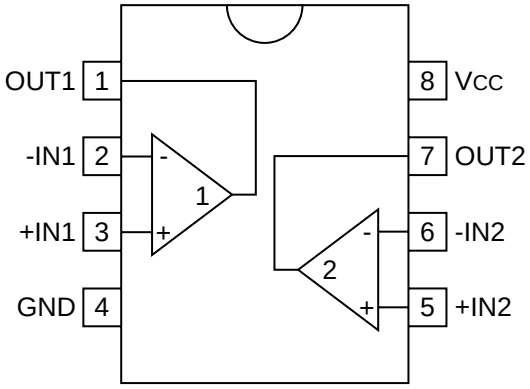
1.Terminal layout



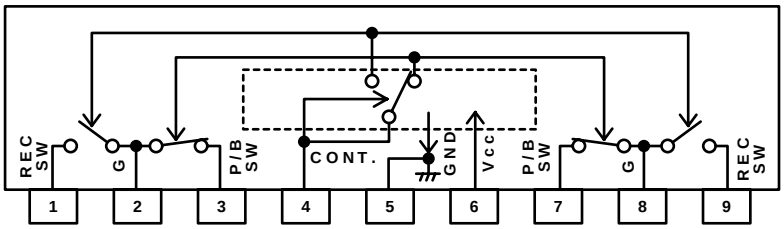
2.Pin function

Pin No.	Symbol	I/O	Function	Pin No.	Symbol	I/O	Function
1	/WE			23	VCC	-	Power supply
2	A19	I	Address input	24	D4	O	Data output
3	A18	I	Address input	25	D12	O	Data output
4	A8	I	Address input	26	D5	O	Data output
5	A7	I	Address input	27	D13	O	Data output
6	A6	I	Address input	28	D6	O	Data output
7	A5	I	Address input	29	D14	O	Data output
8	A4	I	Address input	30	D7	O	Data output
9	A3	I	Address input	31	A0/D15	I/O	Data output/address input
10	A2	I	Address input	32	VSS	-	Connect to GND
11	A1	I	Address input	33	BYTE	I	Mode switch
12	CE	I	Chip enable	34	A17	I	Address input
13	VSS	-	Connect to GND	35	A16	I	Address input
14	DE	O	Output enable	36	A15	I	Address input
15	D0	O	Data output	37	A14	I	Address input
16	D8	O	Data output	38	A13	I	Address input
17	D1	O	Data output	39	A12	I	Address input
18	D9	O	Data output	40	A11	I	Address input
19	D2	O	Data output	41	A10	I	Address input
20	D10	O	Data output	42	A9	I	Address input
21	D3	O	Data output	43	A20	I	Address input
22	D11	O	Data output	44	WP		

■ BA15218 (IC511~IC516, IC534~IC536) : Operation amplifier

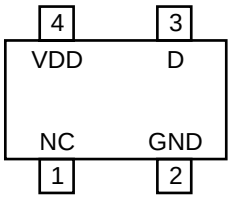


■ BA3126N (IC301) : R/P Switch



■ NAX0393-001 (IC502) : 27MHz Oscilator

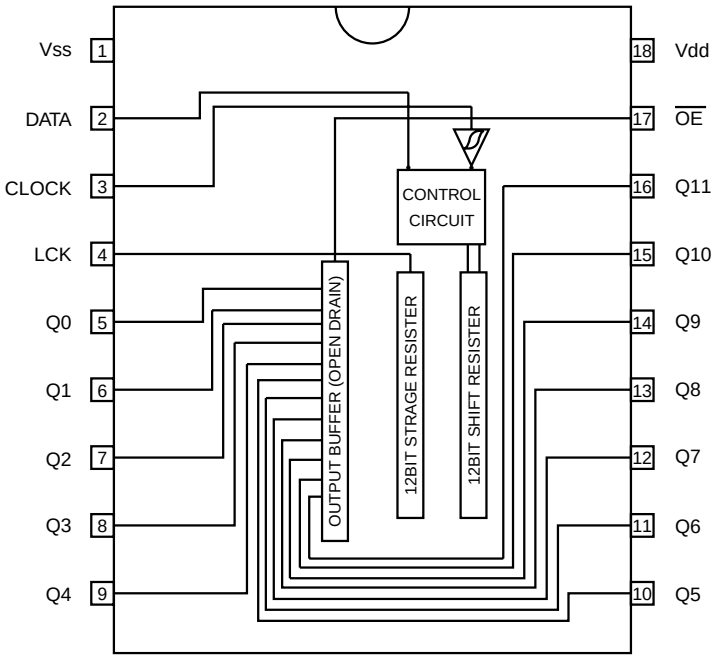
1.Terminal layout



2.Block diagram

■ BU2092BC (IC811) : PORT EXPANDER

1. Terminal Layout

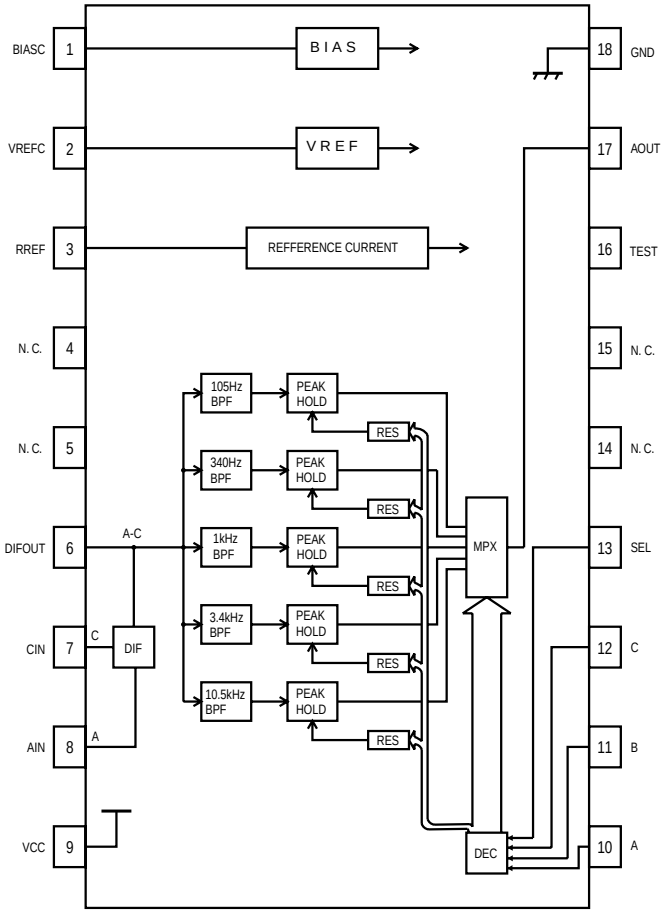


2.Pin function

Pin No.	Symbol	I/O	Function
1	Vss	-	Connect to GND
2	DATA	I	Serial data input
3	CLOCK	I	Shift clock of data
4	LCK	I	Latch clock of data
5~16	Q0~Q11	O	Parallel data output Latch data: L / H OUT PUT: ON / OFF
17	$\overline{OE}$	I	Output enable
18	Vdd	-	Power supply

■ BA3835S (IC812) : SPIIC

1.Terminal layout

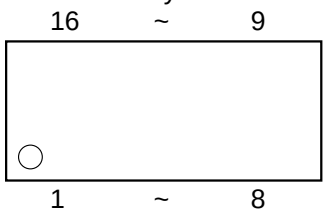


2.Pin function

Pin No.	Symbol	I/O	Function
1	BIASC	I	Connection for decoupplig capacitor that from reference voltage linar section
2	VREFC	I	Connection for decoupplig capacitor that from reference voltage logic section
3	RREF	I	Connection for reference resistor that from band pass filter fo
4	NC	-	Non connect
5	NC	-	Non connect
6	DIFOUT	O	Differntial amplifier output pin
7	CIN	I	Differntial amplifier input pin2
8	AIN	I	Differntial amplifier input pin1
9	VCC	-	Power supply
10	A	I	Output select control pin
11	B	I	Output select control pin
13	SEL	I	Output select control pin
14	NC	-	Non connect
15	NC	-	Non connect
16	TEST	I	TEST signal input
17	AOUT	O	MPX output pin
18	GND	-	Connect to GND

■ BA3838F-X (IC560) : Stero A/D converter

1.Terminal layout

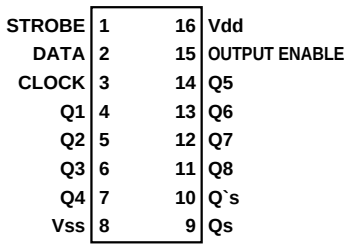


2.Block diagram

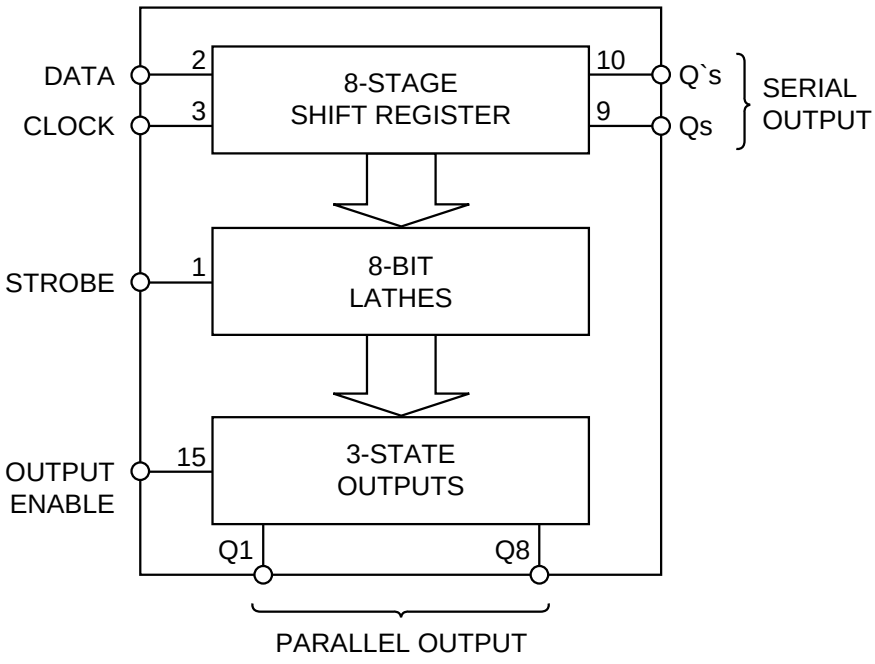
Pin No.	Symbol	I/O	Function
1	VCC	-	Power supply
2	MICIN	I	Microphone mixing input
3	LOUT	O	Channel L output
4	FK	I	Accepts signal from the key controller
5	TK	I	Output signal to the key controller
6	LIN	I	Channel L input
7	BIAS	I	Signal bias
8	GND	-	Connect to GND
9	RIN	I	Channel R input
10	LPF1	I	Connects to LPF time constant element
11	LPF2	I	Connects to LPF time constant element
12	LPF3	O	LPF output
13	ROUT	O	Channel R output
14	CTRLA	I	Mode select input A
15	CTRLB	I	Mode select input B
16	CTRLC	I	Mode select input C

■ BU4094BCF (IC303) : Serial to parallel port extension

1.Terminal layout

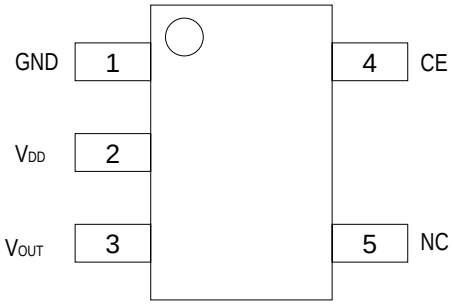


2.Block diagram

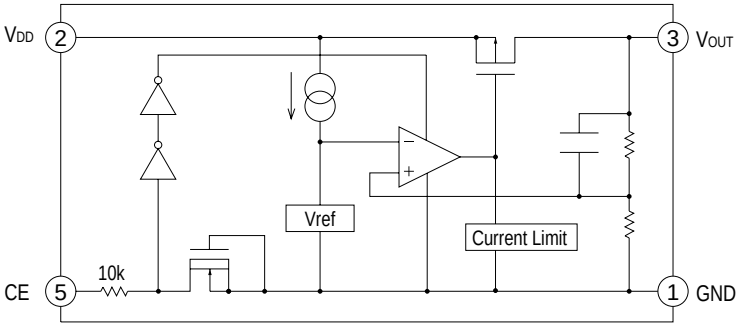


■ MM3023DN-X (IC1, IC102) : Switching regulator

1.Terminal layout



1.Block diagram

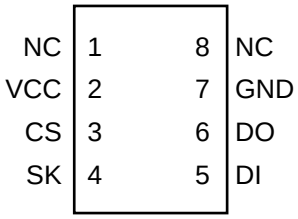


3.Pin function

Pin No.	Symbol	I/O	Function
1	GND	-	Connect to GND
2	VDD	-	Power supply
3	VOUT	O	Regulator output
4	NC	-	No connect
5	CE	I	Output voltage on/off control

■ BR93LC66F-X or AK93C65AF-X (IC403) : EEPROM

1.Terminal layout

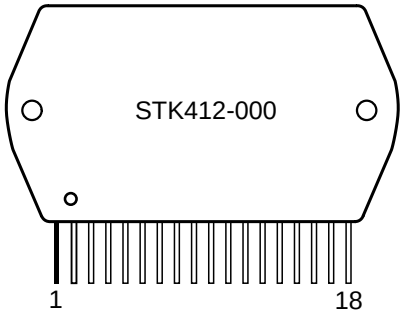


2.Pin Functions

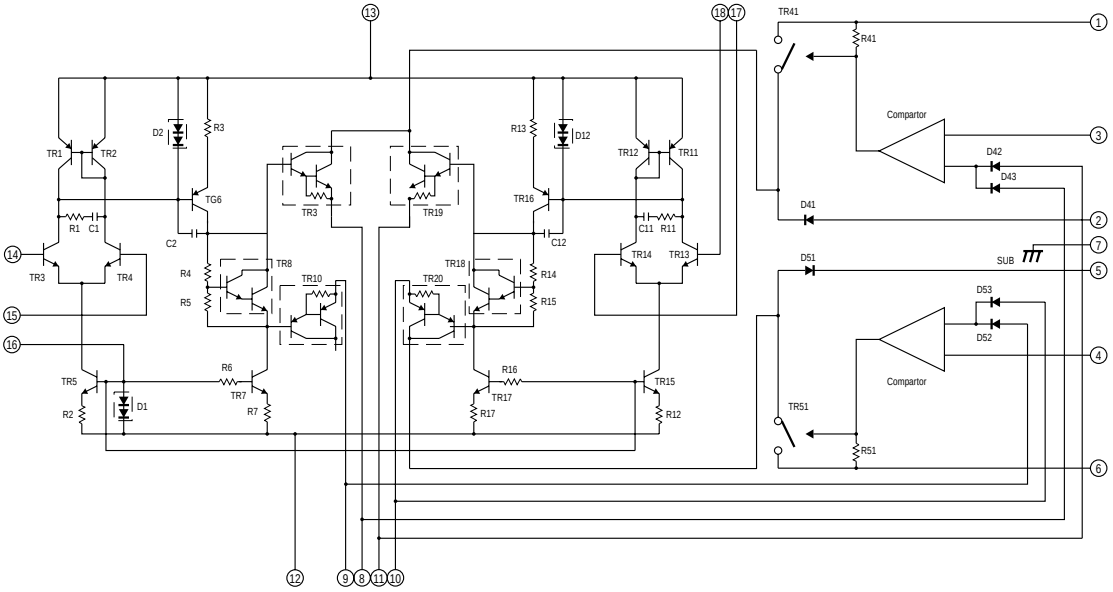
Symbol	I/O	Function
VCC	-	Power supply
GND	-	Connect to GND
CS	I	Chip select input
SK	I	Serial clock input
DI	I	Start bit,OP-code,address,serial data input
DO	O	Serial data output, Internal state display output of READY/BUSY

■ STK412-000 (IC701) : Operation amplifier

1.Terminal layout

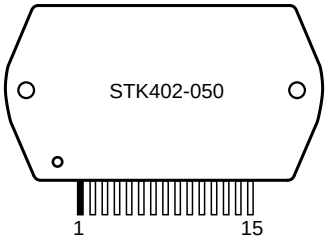


2.Block diagram

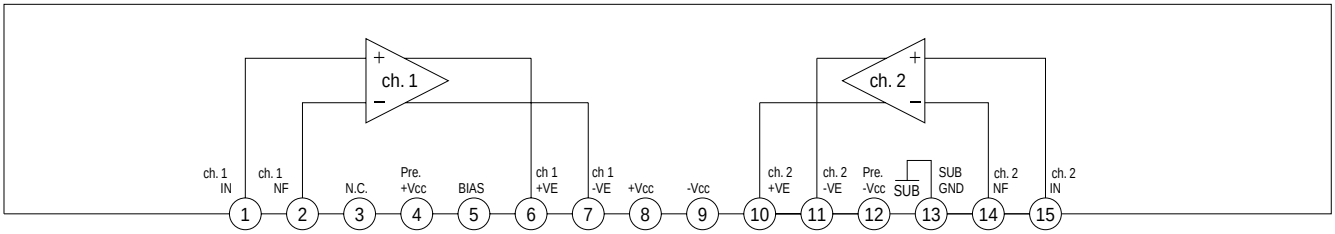


■ STK402-050 (IC752) : Operation amplifier

1.Terminal layout

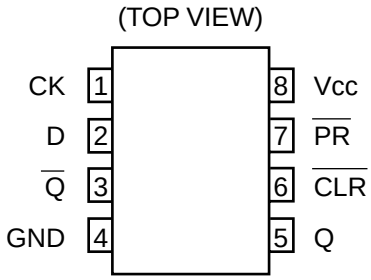


2.Block diagram

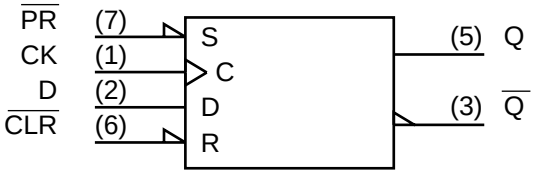


■ TC7WH74FU-X (IC321) : Clock buffer

1.Terminal layout

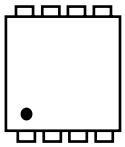


2.Block diagram

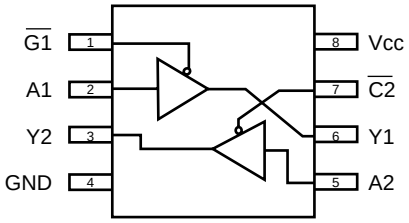


■ TC7W125FU-X (IC412) : Buffer

1. Terminal layout

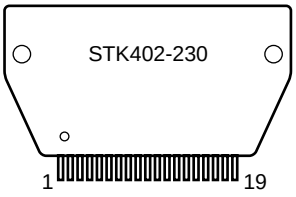


2. Block diagram

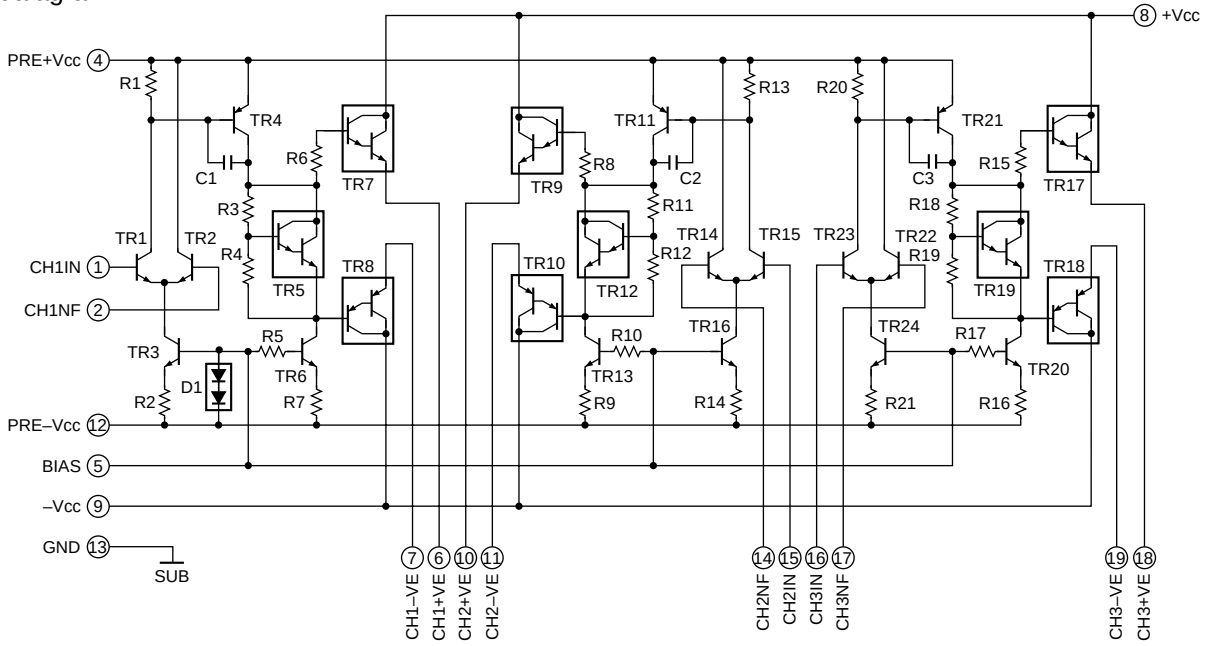


■ STK402-230 (IC107) : Power amp

1. Terminal layout

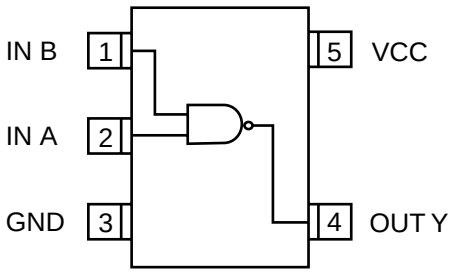


2.Block daiagram



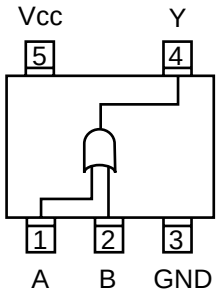
■ TC7SH08FU-X (IC311) : Timing control

1.Terminal layout



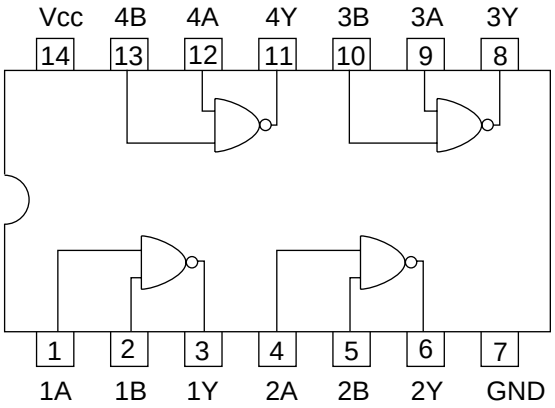
■ TC7SH32FU-X (IC312) : 2 Input Single OR Gate

1.Terminal layout



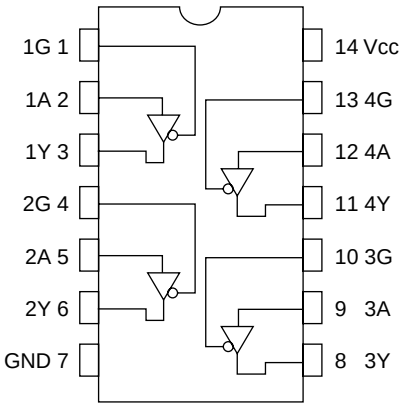
■ TC74VHC00FT-X (IC322,IC503) : Write timing control

1.Terminal layout / Block diagram



■ TC74VHC125FT-X (IC411) : Buffer

1. Pin layout & block diagram



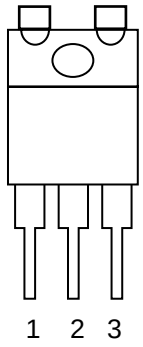
2. Truth table

INPUTS		OUTPUTS
$\overline{G}$	A	Y
H	X	Z
L	L	L
L	H	H

X: Don't care
Z: High impedance

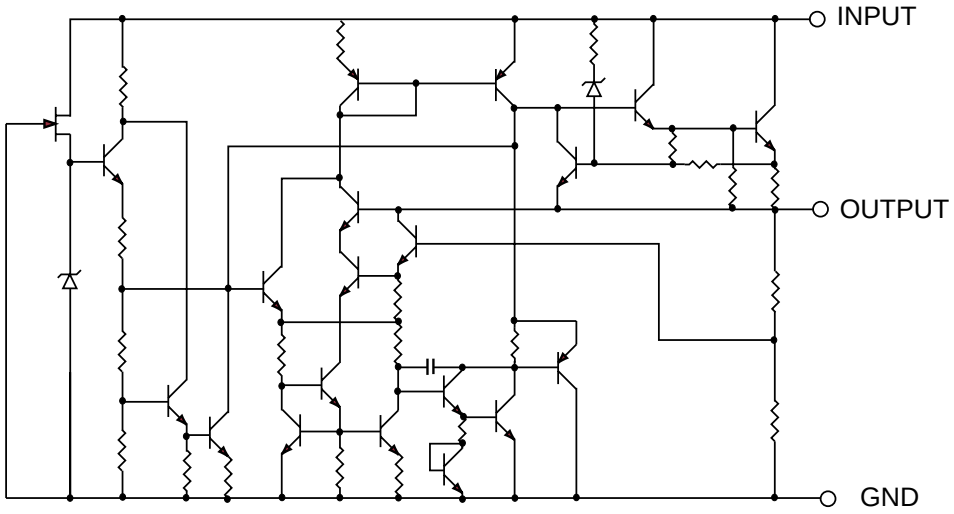
■ NJM78M09FA/NJM78M12FA (IC270/IC271) : Regulator

1.Terminal layout



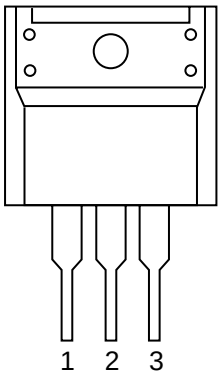
1.INPUT
2.GND
3.OUTPUT

2.Block diagram



■ KIA7805API-T (IC330) : Regulator

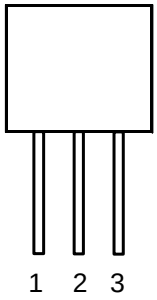
1. Terminal layout



1.VCC
2.GND
3.OUTPUT

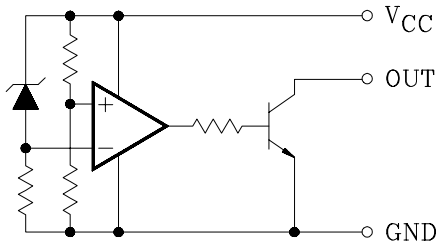
■ KIA7042AP-T (IC830) : Regulator

1. Terminal layout



1.VCC
2.GND
3.OUT

2. Block diagram



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JVC

VICTOR COMPANY OF JAPAN, LIMITED
AUDIO & COMMUNICATION BUSINESS DIVISION
PERSONAL & MOBILE NETWORK BUSINESS UNIT. 10-1,1Chome,Ohwatari-machi,maebashi-city,371-8543,Japan

No.21027

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